Ordering number : ENA0427

SANYO Semiconductors
DATA SHEET

# LV24003LP — Bi-CMOS IC Ultra-compact FM tuner IC for mobile set

## Overview

The LV24003LP is FM tuner IC's that requires absolutely no external components.
They incorporates not only the FM tuner functions but master volume control, tone control, buzzer, source selector, Headphone amp and other functions as well in a compact VQLP package with dimensions of only 5mm×5mm×0.8mm.
These IC's are simply ideal for incorporating FM tuner functions into mobile phones and other small mobile set where space is always at a premium.

## Functions

- FM FE
- FM IF
- MPX Stereo Decoder
- Tuning
- Volume control
- Tone control
- Buzzer
- Source selector
- Headphone amp

## Features

- No external components
- No alignments necessary
- Fully integrated low IF selectivity and demodulation
- Built-in adjacent channel interference total reduction (no 114kHz, no 190kHz)
- Due to new tuning concept, the tuning is independent of the channel spacing
- Very high sensitivity due to integrated low noise RF input amplifier
- Very low power Standby mode. No power switch circuitry required
- MPX output for RDS application
- 3-wire bus interface (Data, Clock, NR-W)
- Digital AFC - Tuner locks to frequency after tuning sequence
- 8 level programmable Soft Mute
- 8 level programmable Stereo Blend
- In combination with the host, fast, low power operation of preset mode, manual search, automatic search and automatic preset store are possible
- Covers all Japanese, European and US bands



SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

## Specifications

### Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{CC}$ max | Analog block supply voltage | 5.0 | V |
| | $V_{DD}$ max | Digital block supply voltage | 4.5 | V |
| Digital input voltage | $V_{IN}1$ max | Clock, Data, NR_W | $V_{DD}$+0.3 | V |
| | $V_{IN}2$ max | External_clk_in | $V_{DD}$+0.3 | V |
| Allowable power dissipation | Pd max | Ta≤70°C | 140 | mW |
| | | Ta≤70°C* | 450 | mW |
| Operating temperature | Topr | | -20 to +70 | °C |
| Storage temperature | Tstg | | -40 to +125 | °C |

* 40mm×50mm×0.8mm Material : glass epoxy resin

### Operating Condition at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Recommended supply voltage | $V_{CC}$ | Analog block supply voltage | 3.0 | V |
| | $V_{DD}$ | Digital block supply voltage | 3.0 | V |
| Operating supply voltage range | $V_{CC}$ op | | 2.7 to 5.0 | V |
| | $V_{DD}$ op | | 2.5 to 4.0 | V |
| | $V_{IO}$ op | Interface supply voltage | 1.8 to 4.0 | V |

Note: Power supply voltage $V_{IO}$ equal $V_{DD}$, or $V_{IO} < V_{DD}$ ($V_{IO} \leq V_{DD}$)

### Interface Conditions at Ta = -20 to +70°C, $V_{SS}$ = 0V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Supply voltage | $V_{DD}$ | | 2.5 | | 4.0 | V |
| Digital part input | $V_{IH}$ | High level input voltage range | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IL}$ | Low level input voltage range | 0 | | 0.6 | V |
| Digital part output | $I_{OL}$ | Low level output current | 2.0 | | | mA |
| | $V_{OL}$ | Low level output voltage $I_{OL}$=2mA | | | 0.6 | V |
| Clock input frequency | fclk | 3wire_bus (29pin) clock frequency | | | 0.7 | MHz |
| External clock frequency | fclk_ext | CLK_IN (31pin) frequency | 32k | | 14M | Hz |

Note: CLK_IN (31pin) can input sign wave.

**Operating Characteristics** at Ta = 25°C, $V_{CC}$=3.0V, $V_{DD}$=3.0V, $V_{OL}$=15, Soft Mute / Stereo=off

$V_{OL}$=15 –Block2 register09h Volume_Bit 3-0 = 0001

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Operational supply current | ICCA | Analog Block at 60dBμ input<br>The 23pin is measured | 15 | 19 | 24 | mA |
| | ICCD | Digital Block at 60dBμ input<br>The 27, 40 pins are measured. | 0.2 | 0.4 | 0.8 | mA |
| Standby supply current | ICCA | Analog standby mode<br>The 23 pin is measured. | | 3 | 30 | μA |
| | ICCD | Digital standby mode<br>The 27, 40 pins are measured. | | 3 | 30 | μA |
| FM coverd frq | F_range | | 76 | | 108 | MHz |
| [FM receiving characteristics ; MONO]: fc=80MHz, fm=1kHz, 22.5kHzdev. soft_stereo, soft_mute, Buss, Treble are all OFF. | | | | | | |
| Input limiting voltage | -3dB LS | $V_{IN}$=60dBμ standard for a -3dB input | | 13 | 22 | dBμV EMF |
| Practical sensitivity | QS1 | for 30dB signal to noise ratio input<br>De-emphasis is 75μs SG open | | 10 | 17 | dBμV EMF |
| Practical sensitivity | QS2 | for 26dB signal to noise ratio input<br>De-emphasis is 75μs SG close | | 1.25 | | μV |
| Demodulator output level | $V_O$ | $V_{IN}$=60dBμ, 11pin output level | 60 | 100 | 140 | mV |
| Channel balance | CB | $V_{IN}$=60dBμ, ratio of 11pin to 12pin output level | -2 | 0 | 2 | dB |
| Signal to noise ratio | S/N | $V_{IN}$=60dBμ, 11pin output level | 48 | 58 | | dB |
| Total harmonic distortion 1(MONO) | THD1 | $V_{IN}$=60dBμ, 22.5kHzdev, 11pin output | | 0.4 | 1.5 | % |
| Total harmonic distortion 2(MONO) | THD2 | $V_{IN}$=60dBμ, 75kHzdev, 11pin output | | 1.3 | 3 | % |
| Field strength level | FS | Input level for FS1 to FS2 | 8 | 18 | 27 | dBμ |
| Muting attenation | Mute-Att | $V_{IN}$=60dBμ, 11pin output level | 60 | 70 | | dB |
| [FM receiving characteristics ; STEREO]: fc=80MHz, fm=1kHz, $V_{IN}$=60dBμV, L+R=30% (22.5kHzdev), Pilot=10% (7.5kHzdev) | | | | | | |
| Separation | SEP | L-mod,11pin→12pin output level | 20 | 35 | | dB |
| Total harmonic distortion (STEREO) | THD-ST | Main-mod (L+R), 11pin/12pin output, IHF_BPF | | 0.6 | 1.8 | % |

**Headphone power characteristics ; LV24003LP** at Ta = 25°C, $V_{CC}$=3.0V, $V_{DD}$=3.0V, fc=1kHz, $R_L$=16Ω,

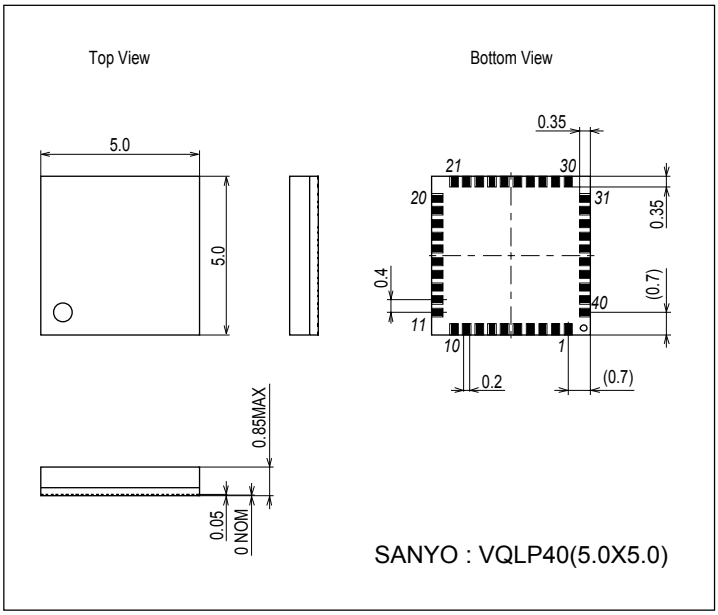
$V_{OL}$= 20 (Max) Line input

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Headphone amp operation supply current | $I_{CC}$_HPA1 | Line input mode. no input | | 3 | 6 | mA |
| Headphone amp standby supply current | $I_{CC}$_HPA2 | Headphone power off mode the 10 pin is measured. | | 3 | 40 | μA |
| HPA power | $P_O$_HPA | THD=10% VR=MAX | 6 | 10 | | mW |
| Total harmonic distortion | THD-HPA | $P_O$=1mW | | 0.6 | 3 | % |
| Output noise voltage | $V_{NO}$ | Rg=10kΩ, BPF=200Hz to 15kHz, VR=14 | | 0.03 | 0.3 | mV |

* VR=Max : Block2 register 09h Volume_Bit3-0 = 0000 setting and Block2 register 07h Volume sgift,bit6= 1 setting

## Package Dimensions

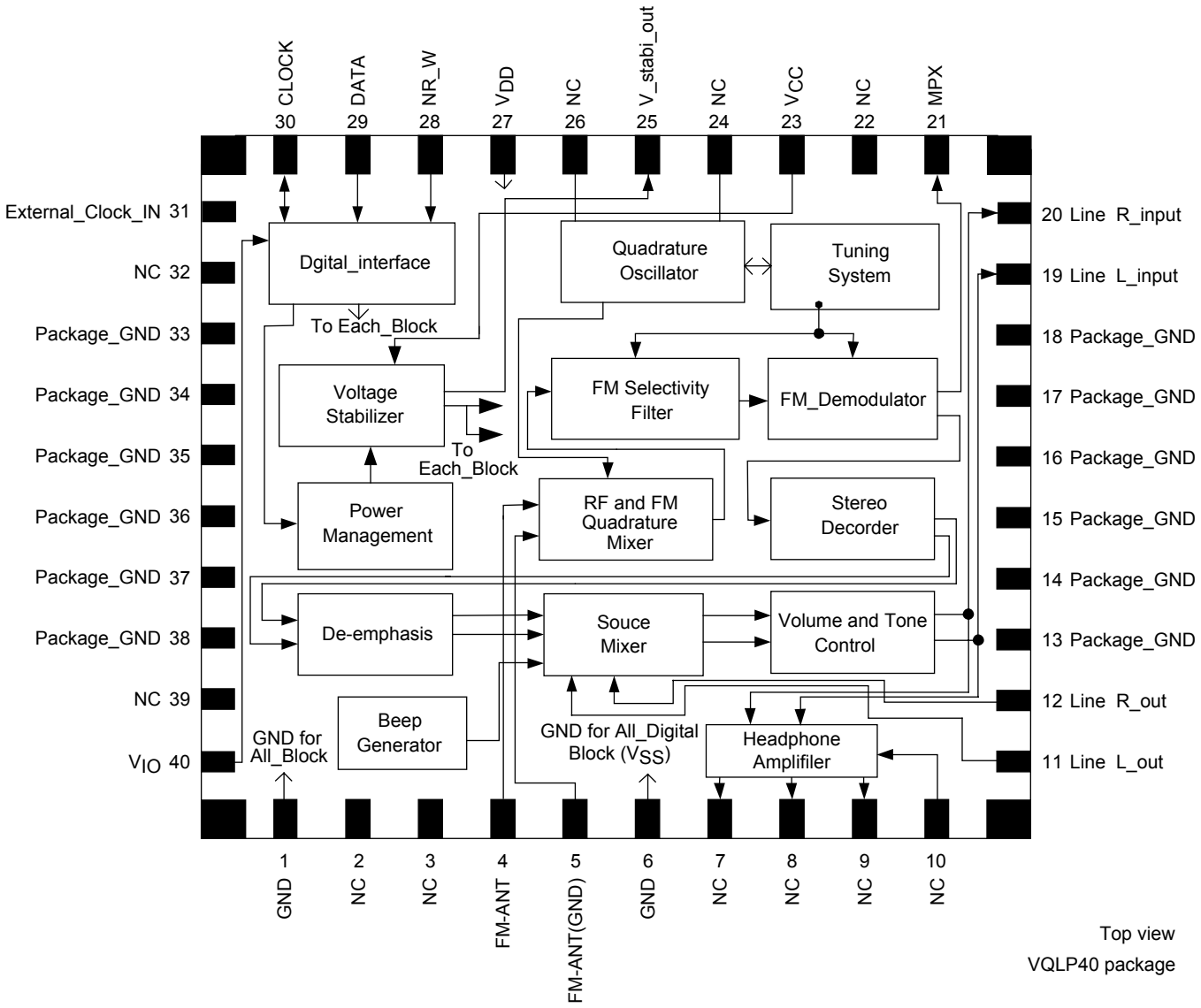
unit : mm (typ)
3302A



## VQLP40 package Pin Description

| Pin | LV24003LP | Description | Remark | DC_bias |
|---|---|---|---|---|
| 1 | GND | GND (Analog and Digital GND) | | |
| 2 | NC | | Do not connect | |
| 3 | NC | | | |
| 4 | FM-ANT1 | Antenna input | | |
| 5 | FM-ANT2 | Antenna GND | Connect to GND | |
| 6 | GND | GND (Analog and Digital GND) | | |
| 7 | HEADPH_R | Headphone Rch output | | 1.2V |
| 8 | HEADPH_C | Headphone common | Not DC GND | 1.2V |
| 9 | HEADPH_L | Headphone Lch output | | 1.2V |
| 10 | $V_{CC}2$ | Headphone supply voltage | | |
| 11 | LINE-OUT-L | Radio Lch Line-output | | 1.2V |
| 12 | LINE-OUT-R | Radio Rch Line-output | | 1.2V |
| 13 | Package-GND | GND for Package-shied | | |
| 14 | Package-GND | GND for Package-shied | | |
| 15 | Package-GND | GND for Package-shied | | |
| 16 | Package-GND | GND for Package-shied | | |
| 17 | Package-GND | GND for Package-shied | | |
| 18 | Package-GND | GND for Package-shied | | |
| 19 | LINE-IN-R | Rch Line-input | | 1.4V |
| 20 | LINE-IN-L | Lch Line-input | | 1.4V |
| 21 | MPX | MPX-signal output | | $V_{CC}$-0.3V |
| 22 | NC | | | |
| 23 | $V_{CC}$ | Analog supply voltage | | |
| 24 | NC(L2) | Internal coil2 | Do not connect | 2.7V |
| 25 | Vstabi. | Stabilizer voltage | | 2.7V |
| 26 | NC(L1) | Internal coil1 | Do not connect | 2.7V |
| 27 | $V_{DD}$ | Digital supply voltage | | |
| 28 | NR_W | Digital interface Read/Write | | |
| 29 | DATA | Digital interface DATA | | |
| 30 | CLOCK | Digital interface Clock | | |
| 31 | CLK_IN | Reference clock-source input for measurement | Connect to GND if not used | |
| 32 | NC | | | |
| 33 | Package-GND | GND for Package-shied | | |
| 34 | Package-GND | GND for Package-shied | | |
| 35 | Package-GND | GND for Package-shied | | |
| 36 | Package-GND | GND for Package-shied | | |
| 37 | Package-GND | GND for Package-shied | | |
| 38 | Package-GND | GND for Package-shied | | |
| 39 | NC | | | |
| 40 | $V_{I/O}$ | Digital interface supply voltage | | |

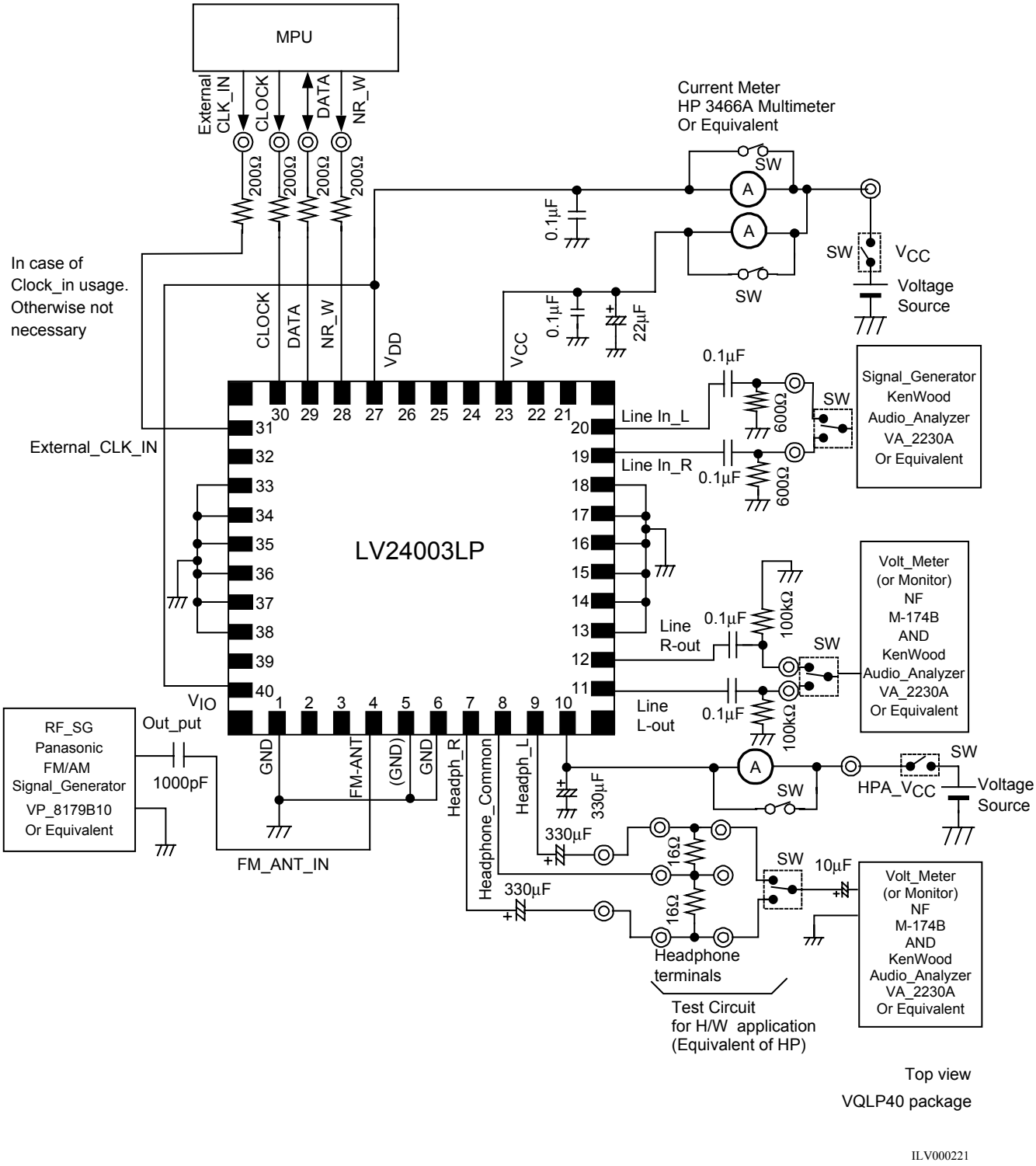
## Block Diagram




Top view
VQLP40 package

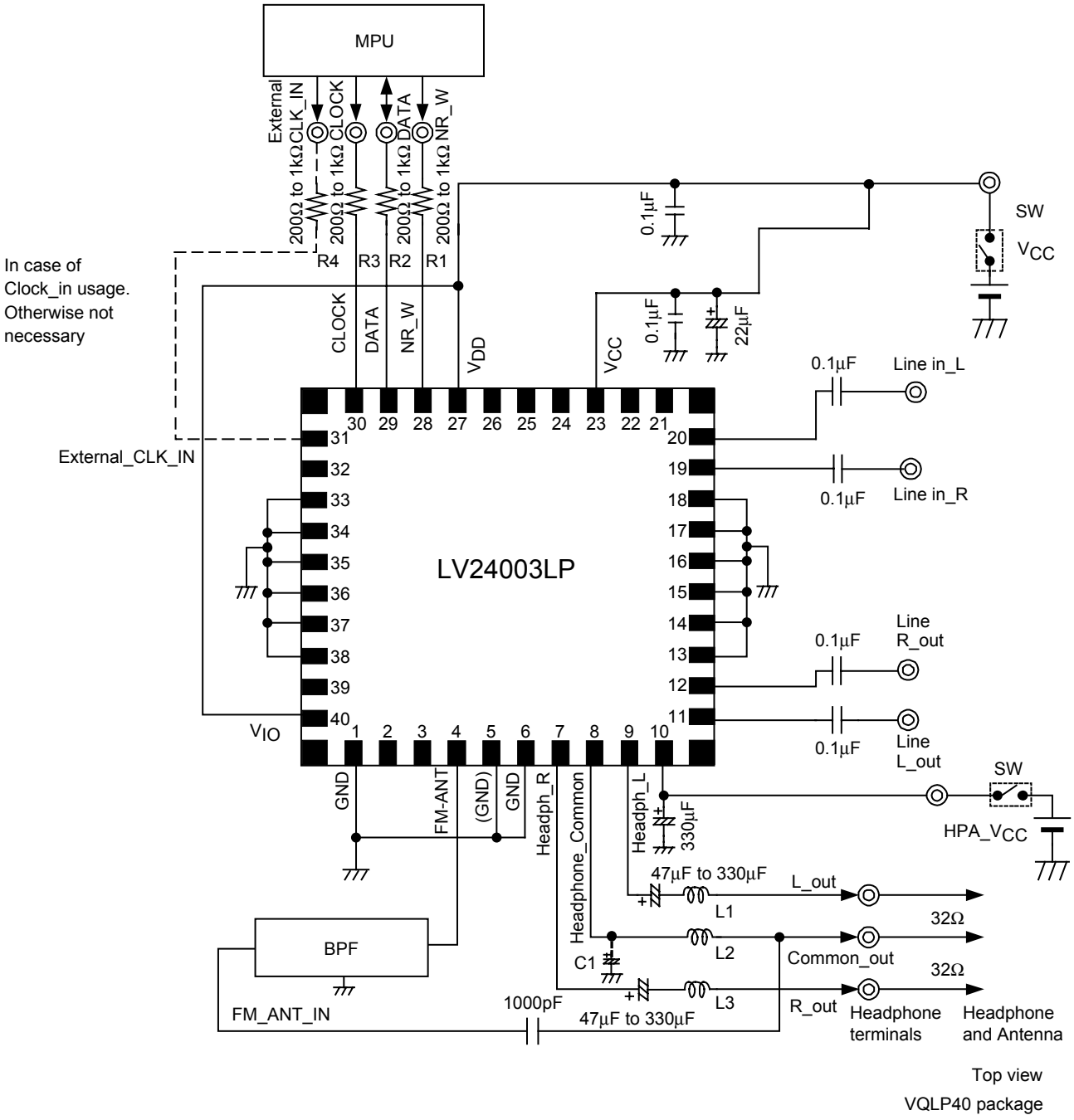
ILV000220

## Measurement Circuit




Note: Pin 13, 14, 15, 16, 17, 18 and Pin 33, 34, 35, 36, 37, 38 are for shield layer-GND of Bottom of Package

## Application Circuit




Note1: Recommend to use 32Ω Headphone
Note2: Recommend to use Value of Inductor (L1, L2, L3) over 820nH for Headphone_output (pin 7, 8, 9)
Note3: In case of not use Headphone for ANT, Please Put Antenna Circuit ceparatly.
Note4: Vale of Extenal Component is just reference. Please set most sutable value under Acutual_operation.
Note5: In case of necessary BPF, Please put Between FM_ANT and HPA
Note6: We recommend to put C1 (100µF to 220µF) to Pin 9 for AC_GND
Note7: We recommend to put R1, R2, R3, R4 for interface_wire.
Note8: Please put Capacitor Between $V_{DD}$ and GND also, put Capacitor Between $V_{CC}$ and GND as shown on application.
Note9: Pin 13, 14, 15, 16, 17, 18 and Pin 33, 34, 35, 36, 37, 38 are for shield layer-GND of Bottom of Package