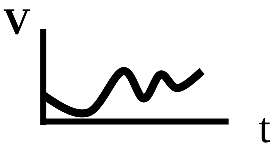
Digital Integrated Circuits (Gates and Flip-Flops)

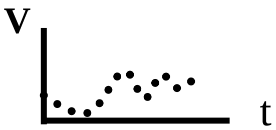
PHYS 333-334 LAB-D1

Produced by N. Abbasi from notes by G. Palmer

Digital Circuits



- **analog:** transducer outputs (continuous)



- **digital:** discrete levels
- **digital advantages -** noise (transmission), arithmetic (Boolean)

- **Gates and flip flops -** building blocks of ICs, Memories
- **Logic Families**
  - **TTL -** Transistor Transistor Logic **-** original (TI, 1964), cheap, rugged, (~10mW/gate)
  - **CMOS** – Complementary Metal Oxide Semiconductor
    - High speed, low power, static electricity

  - Power Supply → 5V (NOT 15V!!!)

TTL and CMOS Logic Families

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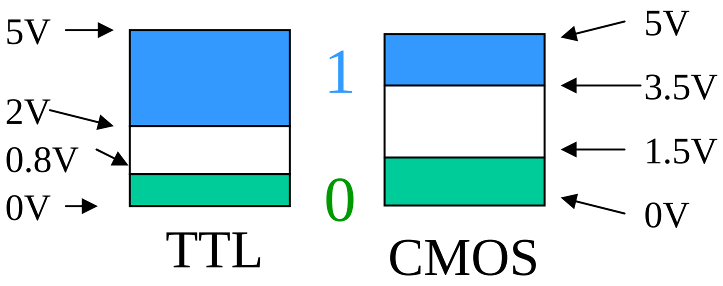
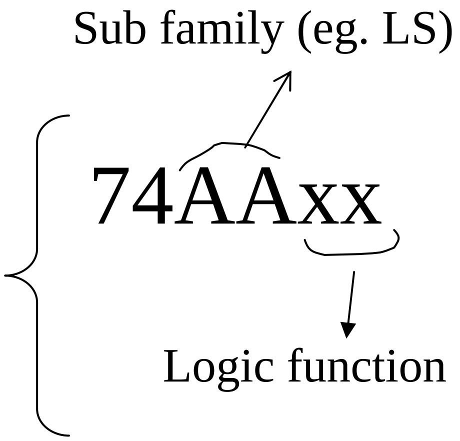
binary logic: '1' is true or more positive voltage level,
'0' is the false or less positive voltage level

Logic Levels in TTL and CMOS

Logic Family **Logic Level**	**TTL**	**CMOS**
HIGH (1)	2 to 5V	3.5 to 5V
LOW (0)	0 to 0.8V	0 to 1.5V
indeterminate	0.8 to 2V	1.5 to 3.5V



7400 → NAND Gate
7486 → XOR Gate

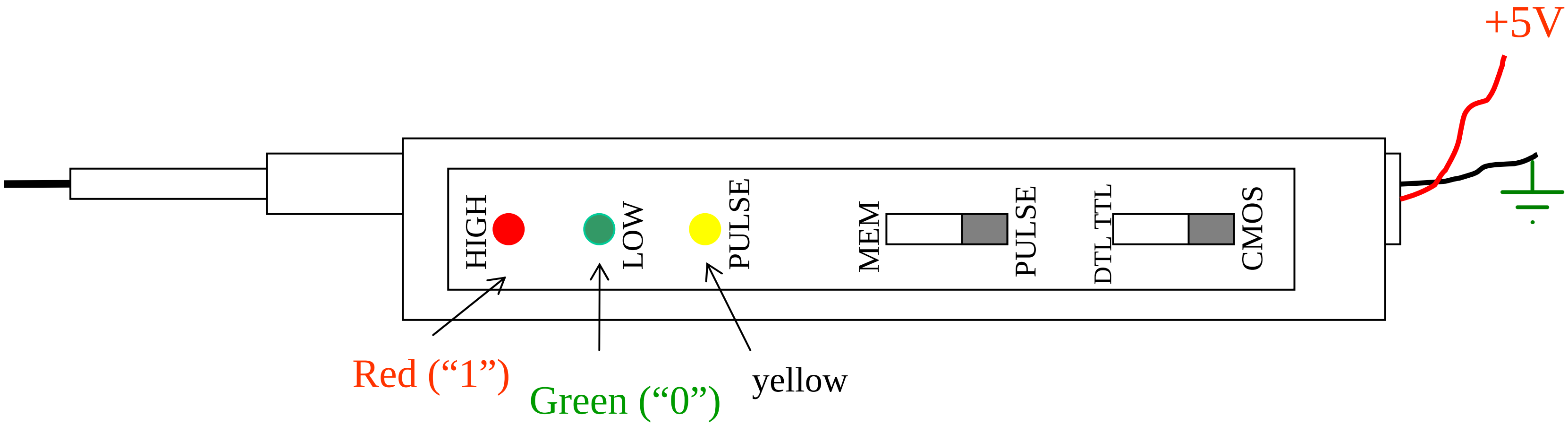


Logic Indicator
(diagnostic tool)

ILC: eight "logic" LEDs on board - on indicates "1"

- off indicates "0"

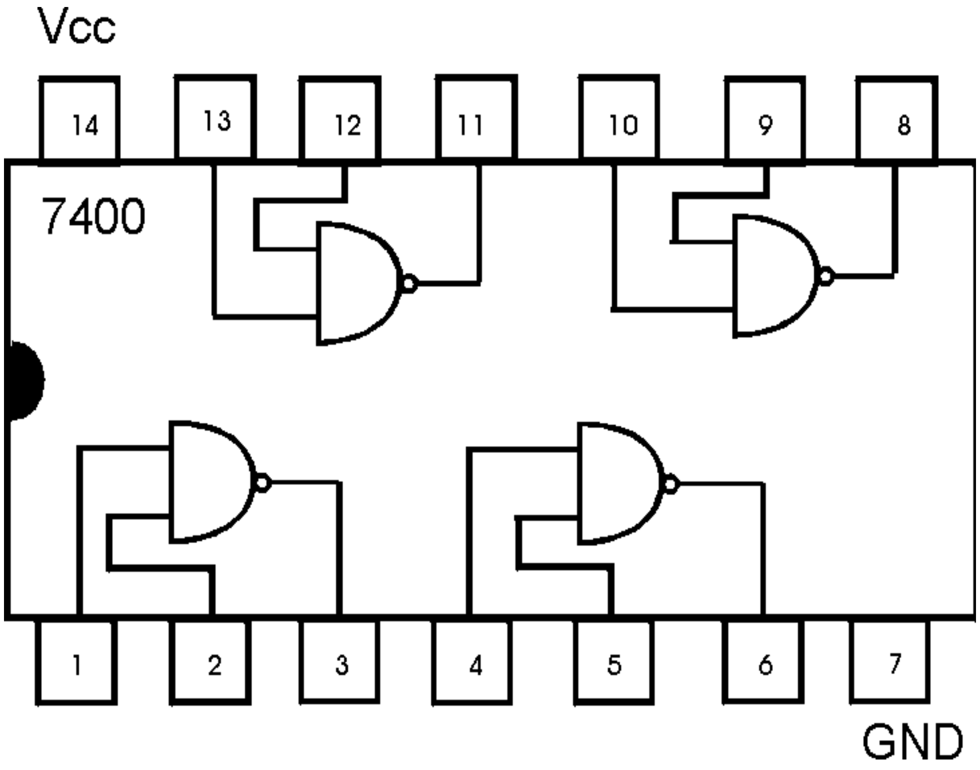
Stirling: Logic Probe



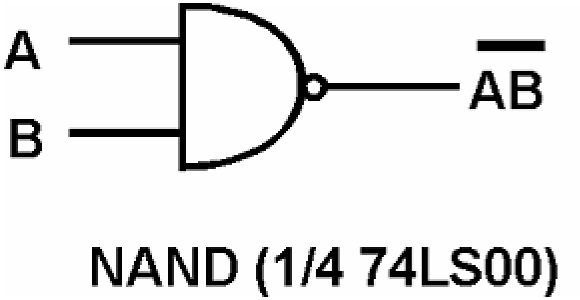
GATES

GATES: - immediate output determined only by inputs

1) NAND



PIN diagram



Logic Symbol

Experimental Work: Gates

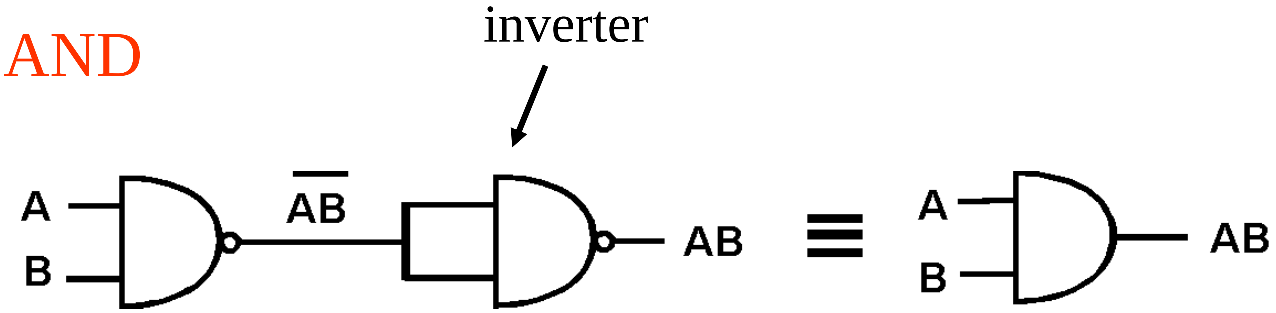
- Connect up one TTL NAND (ie 74LS00) gate
- measure the logic and voltage levels for the the truth table
- Repeat with one CMOS NAND (ie 74HC00)

Table D1.1 (modified)

Input A (Logic)	Input A (V)	Input B (Logic)	Input B (V)	Output $\overline{AB}$ (Logic)	Output $\overline{AB}$(V)	
					TTL	CMOS
0		0				
1		0				
0		1				
1		1				

Gates cont'd

2) AND



1. **Note:** NAND gates can be used to implement other logic functions
2. Build an AND gate using two NAND gates
3. Apply logic signals to the inputs of the gate and complete the truth table

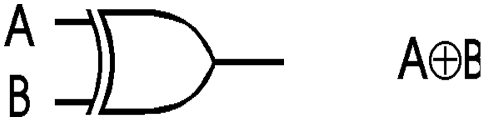
Logic Input A	**Logic Input B**	**Logic output AB**
0	0	
1	0	
0	1	
1	1	

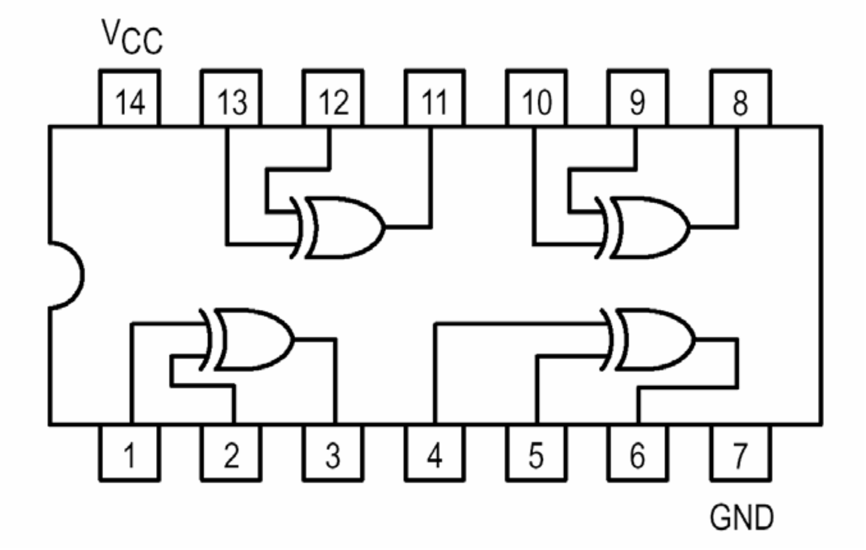
Gates cont’d

3) XOR (“exclusive or”)

- 7486 same pin diagram as 7400 NAND

Logic Symbol





7486 PIN diagram

XOR Truth Table

A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Gates cont’d

MSB LSB

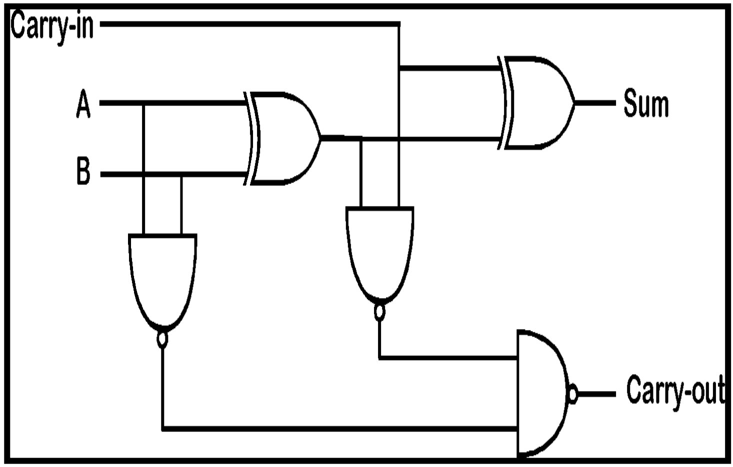
Binary Numbers: 1 1 0 1 (binary) =13 (decimal)

2^3 2^2 2^1 2^0 10^1 10^0

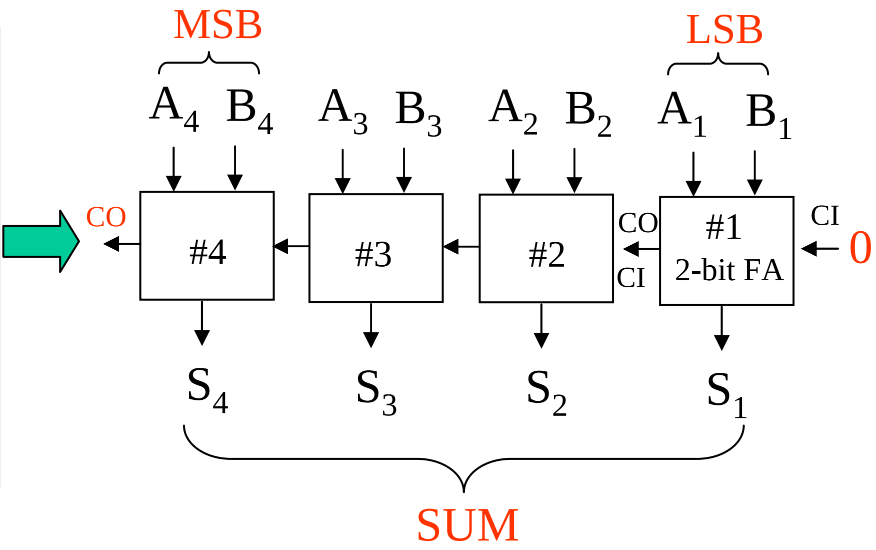
Experimental - make “2-bit” full adder with XORs, NANDs

Note: multi-bit numbers are added by 2-bit adders in tandem

2-bit Full Adder



4-bit Adder (A+B)



Gates cont’d

Experimental Work

1. Build the full adder
2. Complete the truth table
3. Show **logic** in adder on **handout** for $(C_{in},A,B)=(1,1,1)$

Full Adder Truth Table

2^1 2^0

A	**B**	**Cin**	**Cout** (MSB)	**SUM** (LSB)
0	0	0		
1	0	0		
0	1	0		
0	0	1		
1	1	0		
0	1	1		
1	0	1		
1	1	1		

Produced by N. Abbasi from notes by G. Palmer

Handout (Logic Worksheet)

Fig D1.4
Binary 2-bit Full Adder

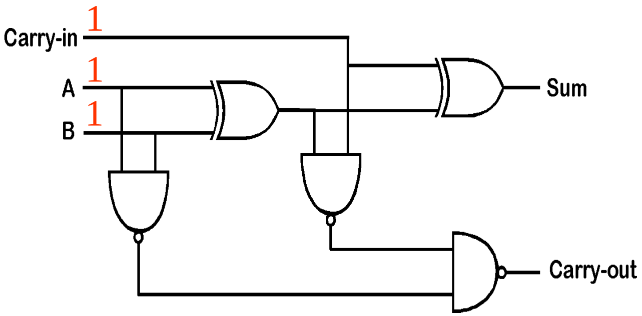
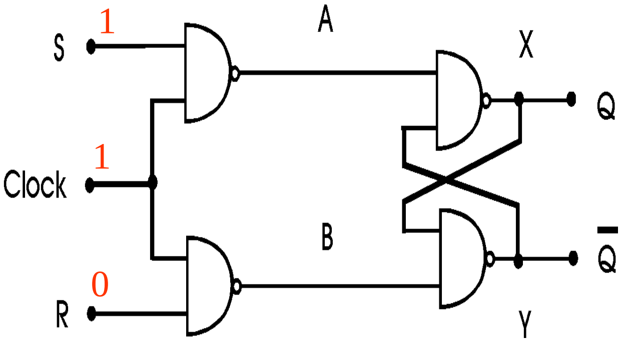
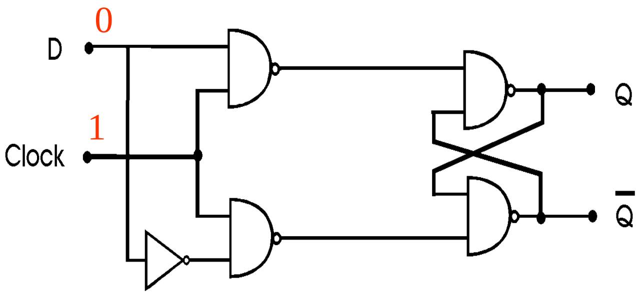


Fig D1.6
Clocked RS Flip Flop



		XOR	NAND
A	B	$A \oplus B$	$\overline{AB}$
0	0	0	1
1	0	1	1
0	1	1	1
1	1	0	0

Fig D1.7
D Flip Flop
(Text:Sect.13.2.3)

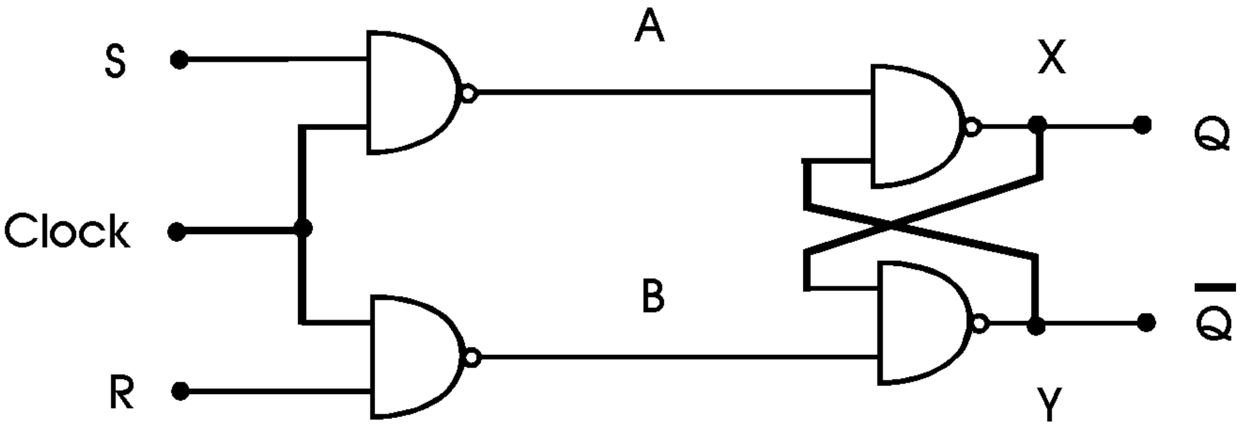


FLIP FLOPS (bistables)

- output is determined by inputs and history → memory and delay

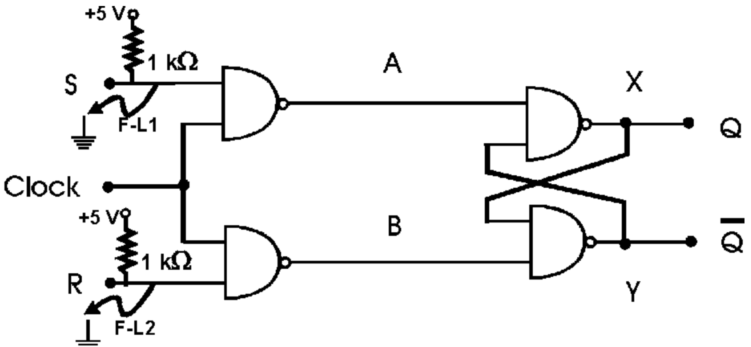
Reset Set

1) Clocked RS Flip Flop



Experimental Work

1. Build the RS Flip flop, and construct the truth table
2. Explain why S=R=1 is indeterminate
3. Show **logic** in RS Flip Flop circuit on **handout** for “set” state (C,S,R)=(1,1,0)
4. Complete the **timing** diagram on the **handout** for RS flip flop



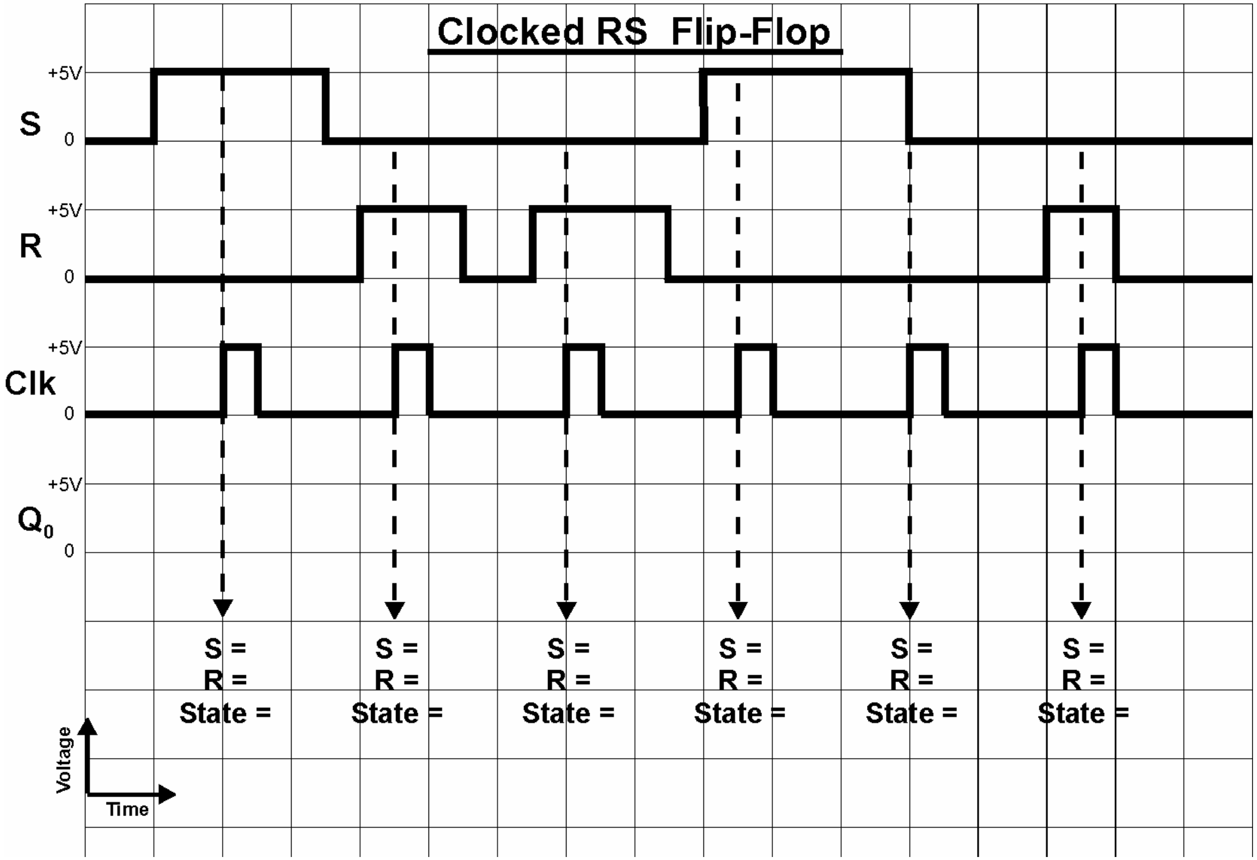
For the case of R = S = 1, connect F-L1 from S to R and disconnect F-L2 from Ground.
To return to case R = S = 0, now connect F-L2 to Ground

Fig D1.6 RS Flip Flop Truth Table

Memory

	C	S	R	at S,R Q	at S,R $\bar{Q}$	S,R returned to (0,0) Q	S,R returned to (0,0) $\bar{Q}$
	1	0	0				
Set State →	1	1	0				
Reset State →	1	0	1				
Indeterminate →	1	1	1				
	0	x	x				

PHYS 333 - 334 -- Lab D1 Timing Diagram for Flip -Flops

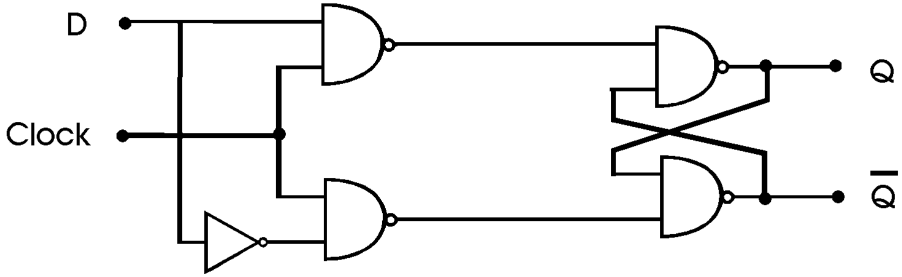


Flip Flops cont'd

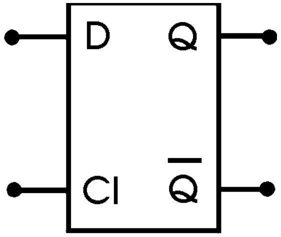
3) D Flip Flop (Data latch) – <u>for information only</u>

- Indeterminate state of the RS flip-flop eliminated with the D-type flip-flop

- D flip flop can store and delay data

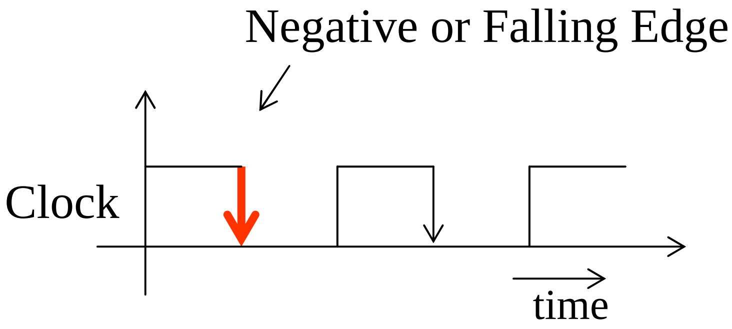


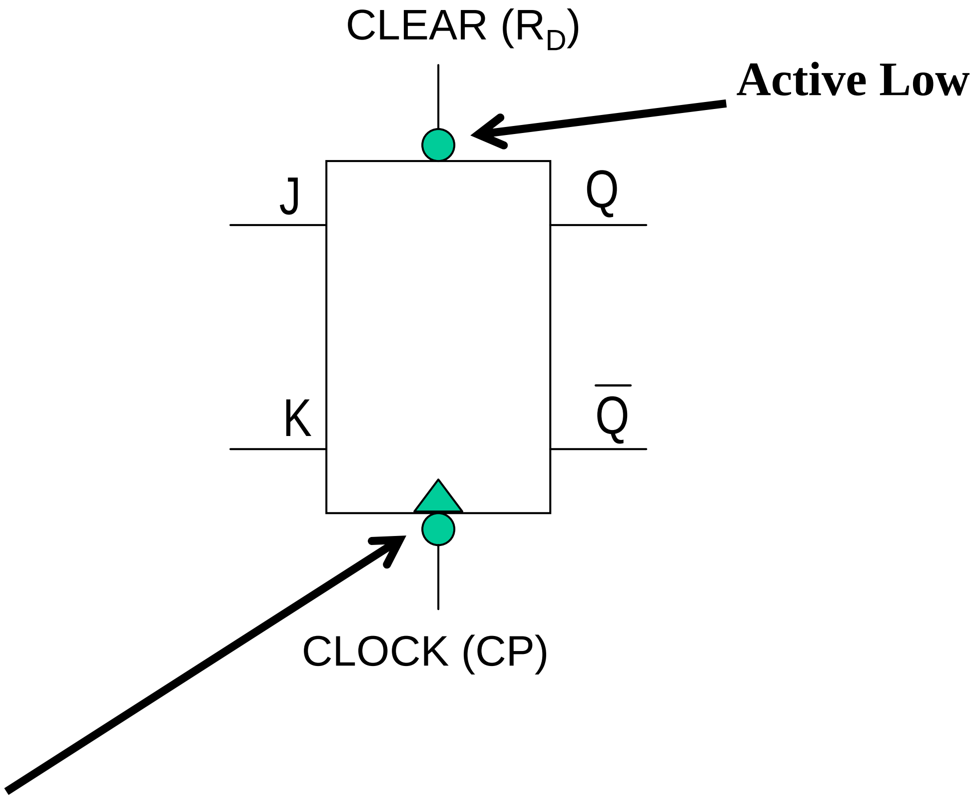
Logic Circuit



Logic Symbol

JK Flip Flop


Negative or Falling Edge



Active Low

74LS73 - Dual **Negative Edge-Triggered** J-K Flip-Flop with Clear

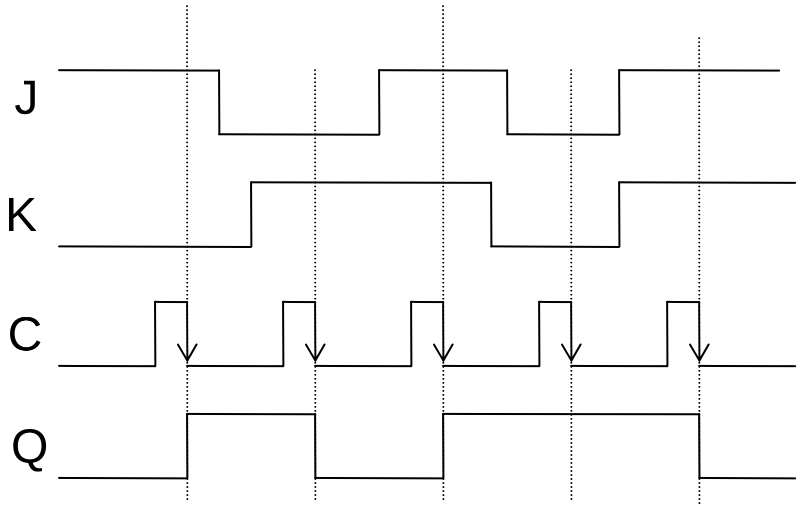
Produced by N. Abbasi from notes by G. Palmer

JK Flip Flop

Function Table

J	K	C	Q
1	0	↓	1
0	1	↓	0
1	1	↓	$Q_{n+1} \rightarrow Q_n$
0	0	↓	No change

Timing diagram



J = 1
K = 0
SET

J = 0
K = 1
RESET

J = 1
K = 1
TOGGLE

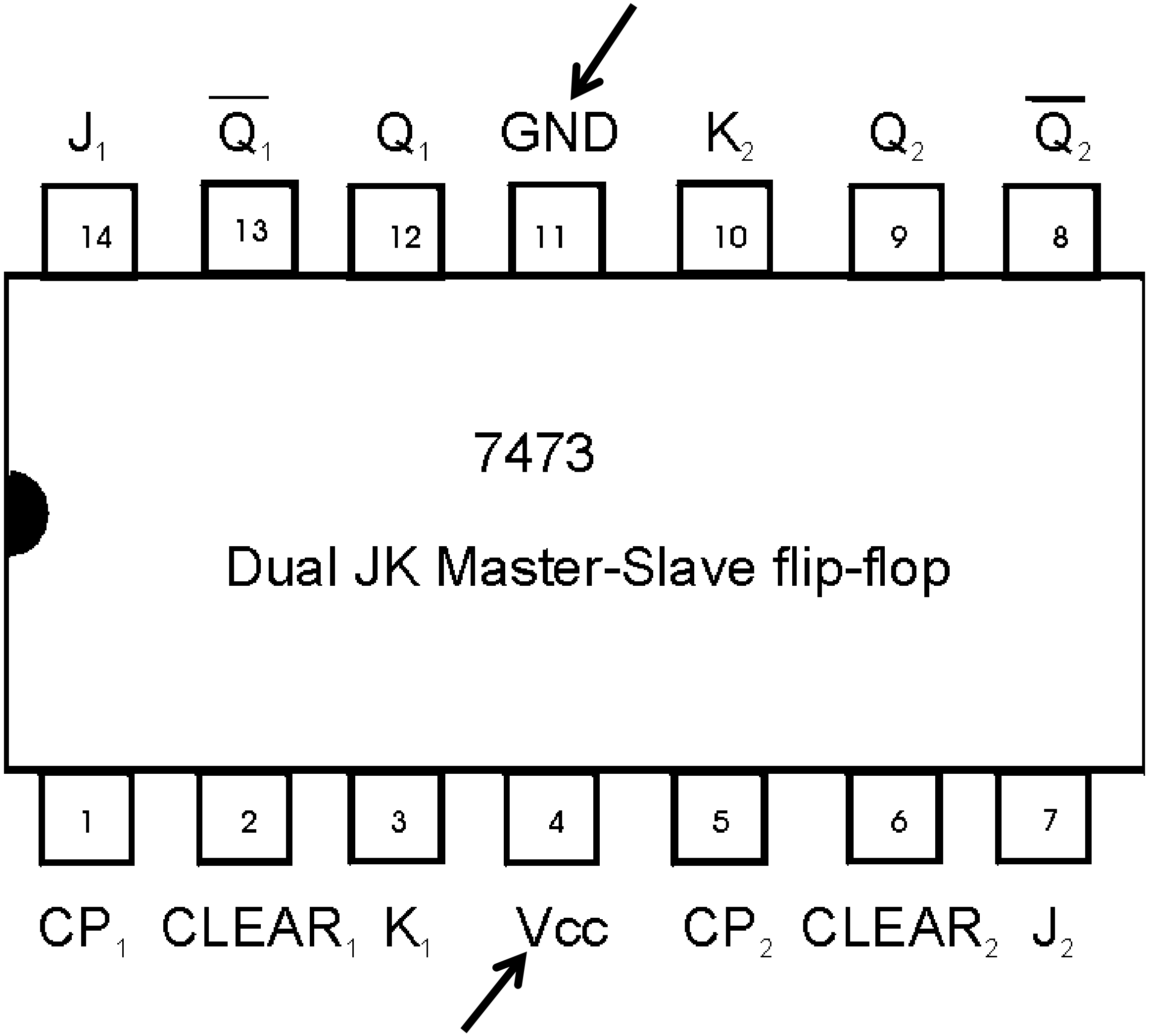
J = 0
K = 0
NC

J = 1
K = 1
TOGGLE

Toggle (ie ÷2) ← Useful for counting

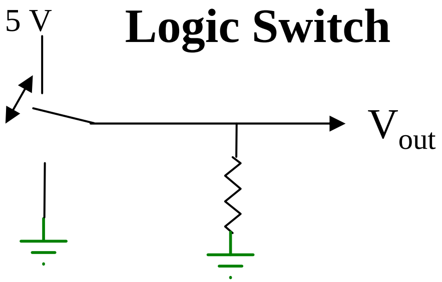
74LS73

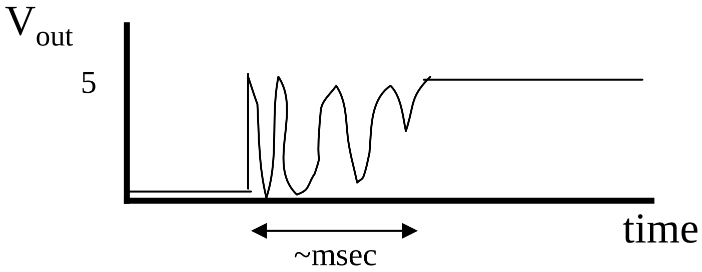
Pin diagram

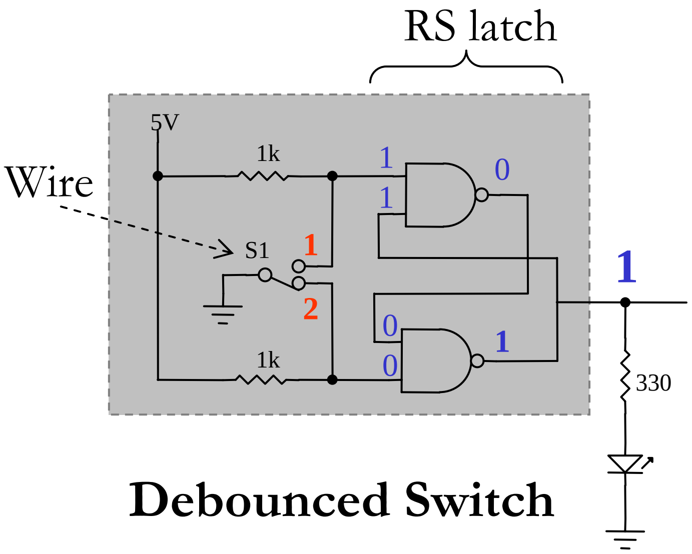


Single Pulse Clock
(switch debouncer)

Logic Switch



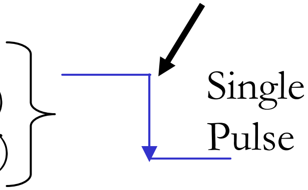




Debounced Switch

S1 at 2 → CLK = “1” (LED on)
S1 at 1 → CLK = “0” (LED off)

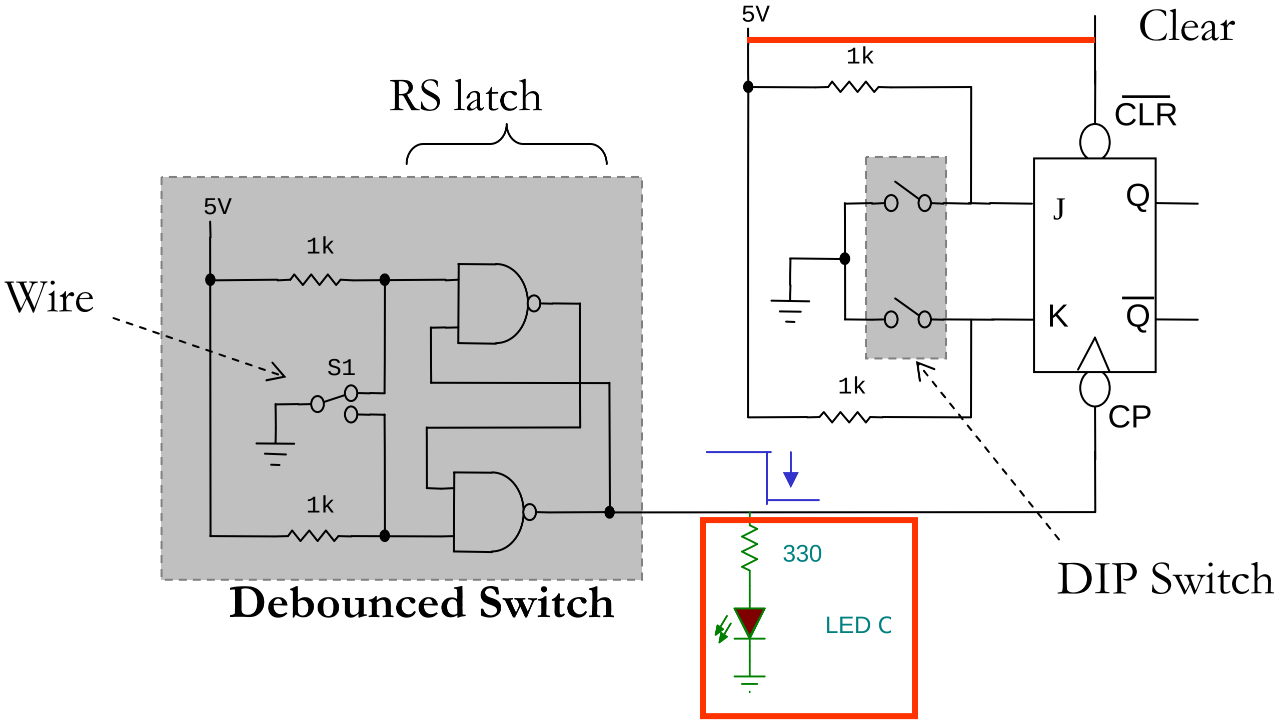
Falling edge of clock

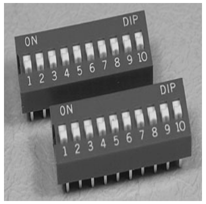


Experimental Work

1. Build the logic circuit
2. Verify the truth table using single clock pulse
3. Observe the “toggle” state – (i.e. J=K=1)
4. Observe that the negative edge of the clock (ie ↓) changes Q

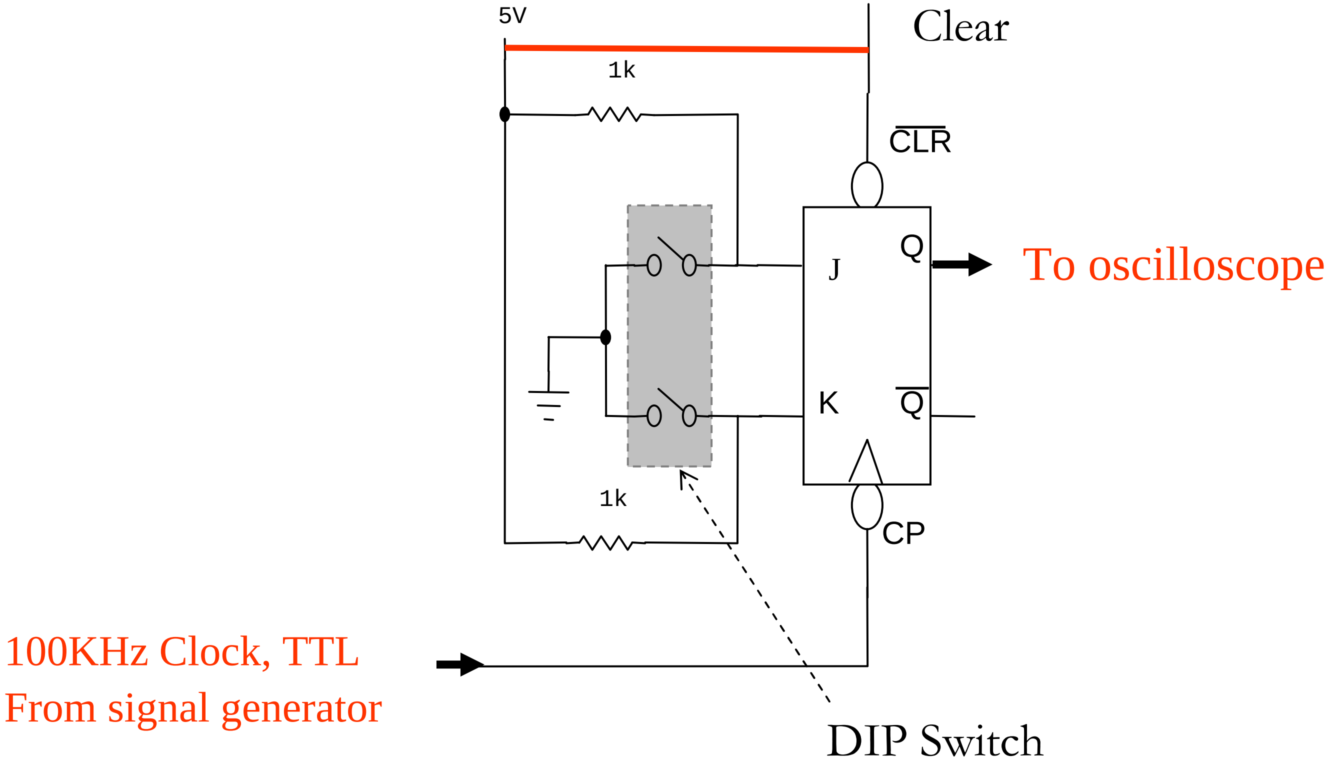
Fig D1.7

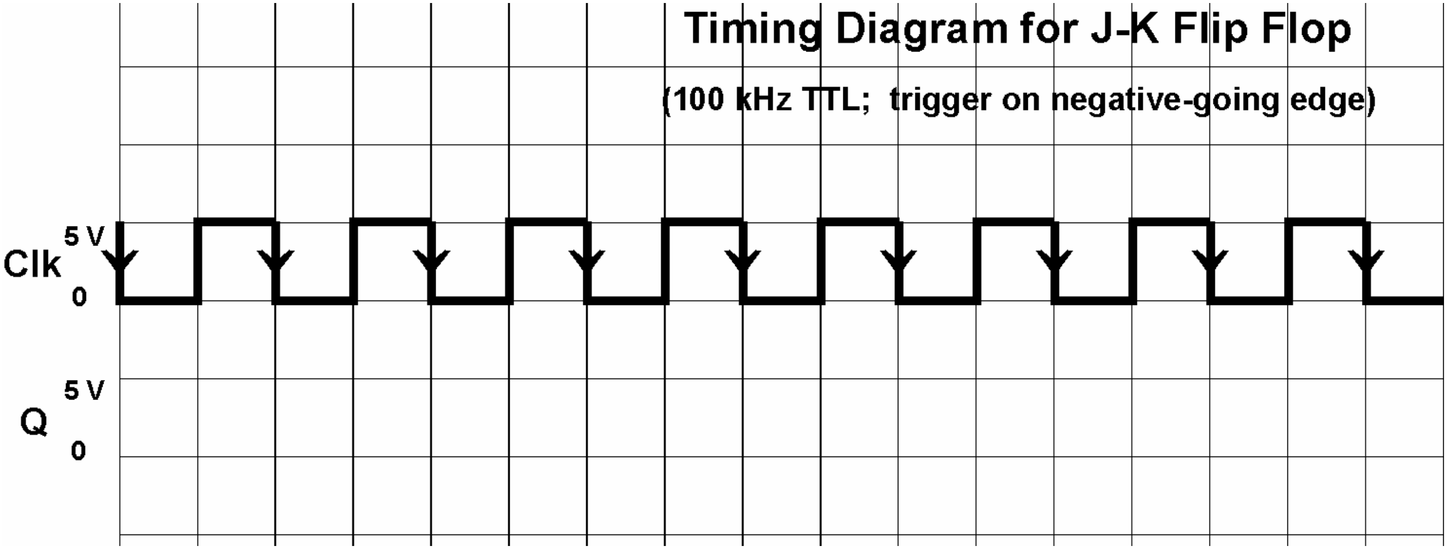




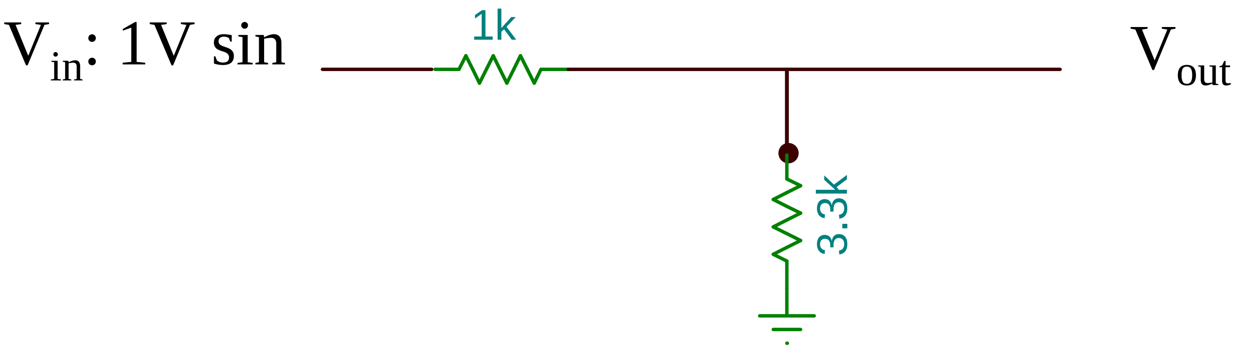
Experimental Work cont'd

5. Sketch Q (from oscilloscope) on the **timing diagram** using 100KHz **TTL** pulses as the clock. Use toggle state (J=K=1)




Timing Diagram for J-K Flip Flop
(100 kHz TTL; trigger on negative-going edge)
Clk
5 V
0
Q
5 V
0

Typical Lab Test Question



V_{in}: 1V sin

V_{out}

Problem: measure gain (in db) at 1 kHz

Time limit 4 min