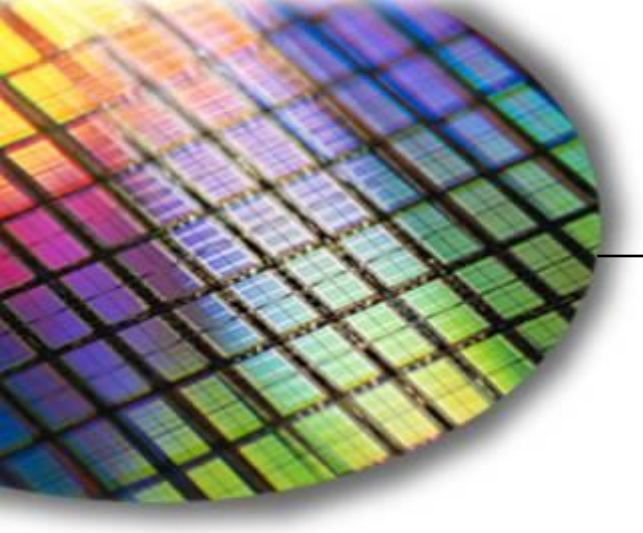


The World Leader in High Performance Signal Processing Solutions

Driving High Performance ADCs in Communication Applications

Carlos Calvo
Analog Device
June 2008

ANALOG DEVICES

Agenda

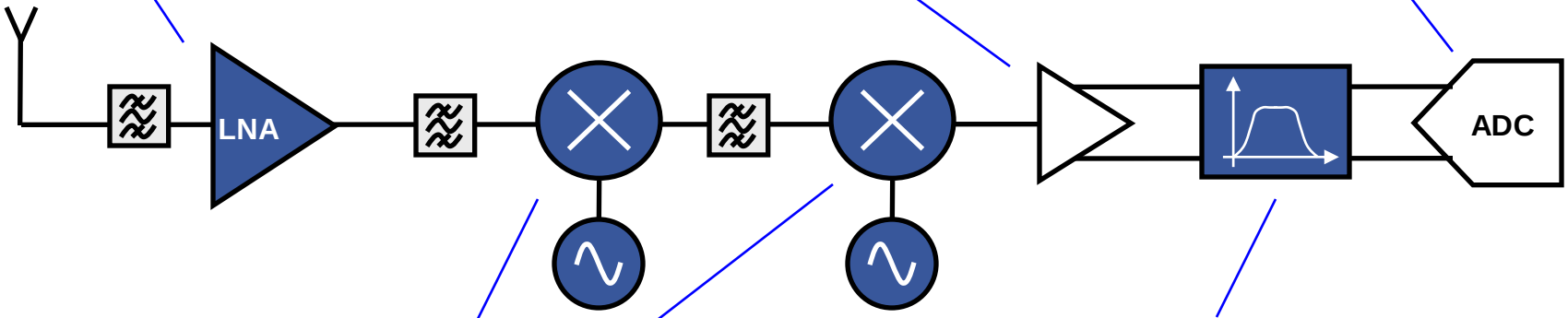
- Communications System Overview
- System Performance Metrics
- RF versus ADC terminology
- System budgeting
- Different ADC driver implementations
- Filter design considerations and techniques
- Single-ended versus Balance Drive
- Driver interface examples

Traditional Receive Architecture

Low Noise Amplifier:
Increase signal amplitude with minimum degradation of noise floor

ADC Driver:
Prepare the signal to be digitized, converting, offering gain and sometimes providing single-ended to balanced conversion

ADC:
Digitize baseband information



Mixers:
Frequency translate the signal of interest, down-converting the high frequency to a lower frequency

Anti-Aliasing Filter:
Limit the bandwidth of the noise at the ADC input and suppress out of band spurious components still in the signal path. Low pass for direct conversion or bandpass for IF Conversion.

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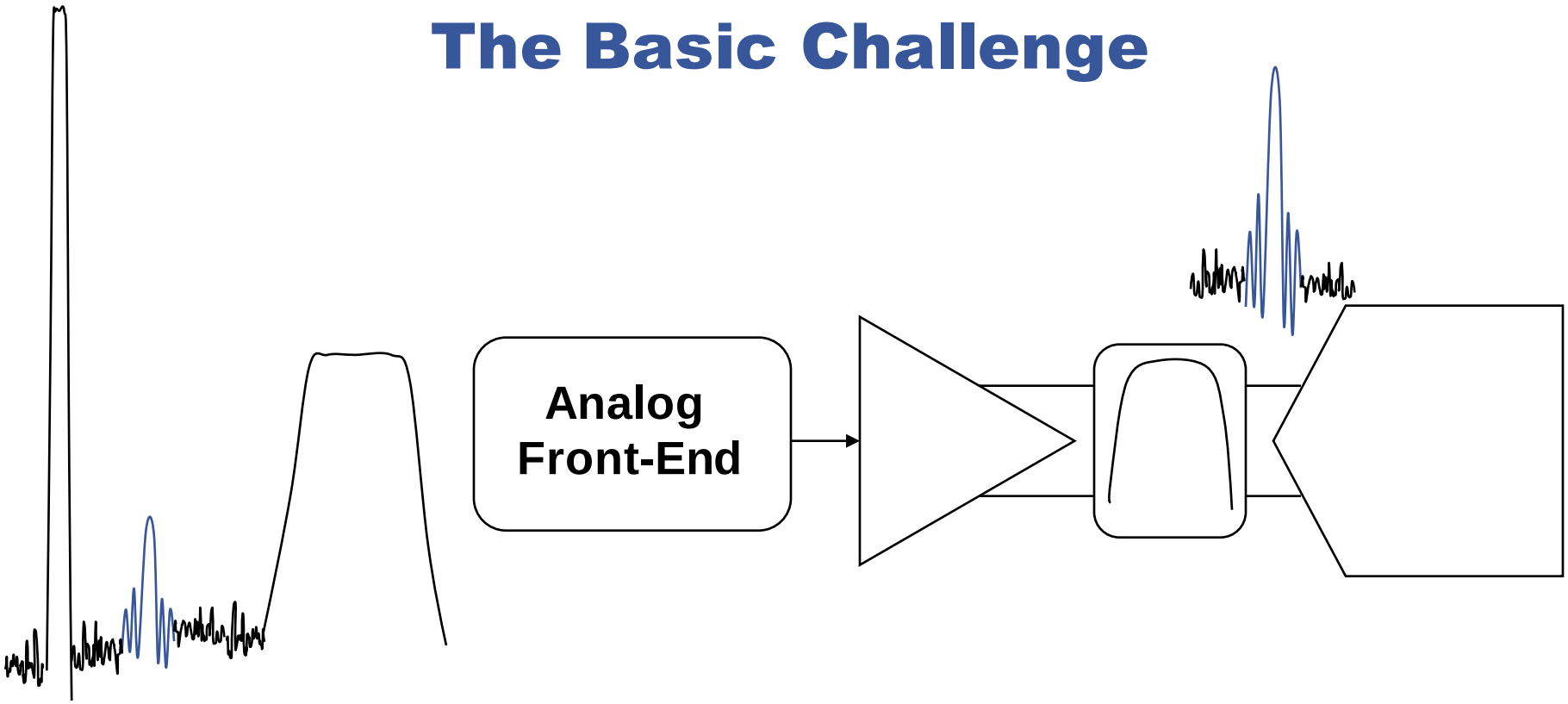
Communication Systems Considerations

What makes for a good radio design?

- Good Sensitivity
  - Low NF
  - Low Synth and Clock phase noise
- Sufficient input signal level handling capacity
  - High input IP3 and IP1dB
- Robust performance under blocking
  - High Input Linearity
  - Good Selectivity
  - Good NF immunity under large signal
- Other Considerations
  - Low-Cost
  - Low-Power
  - Compact

The Basic Challenge



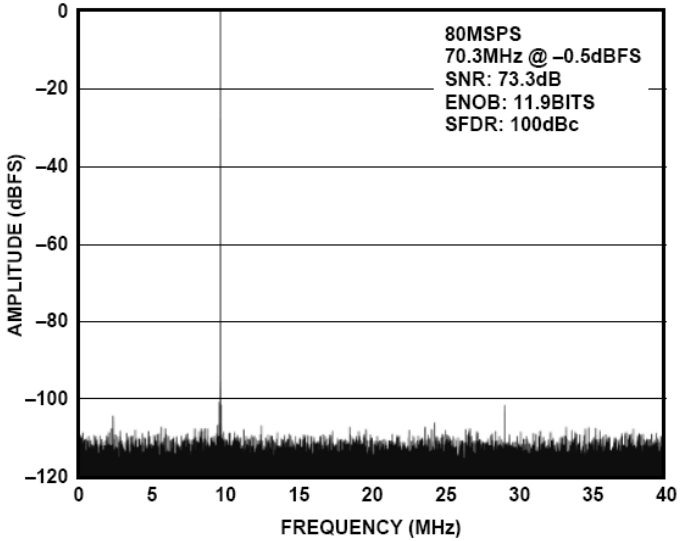
Need to successfully drive wanted signal into ADC with adequate fidelity for signal detection. Requires proper component selection and interface implementation.

System Performance Metrics

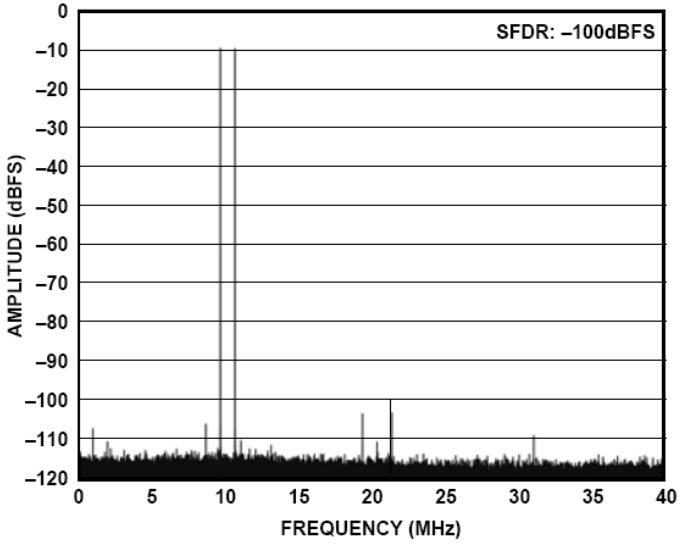
- **Noise Figure** is a useful metric to describe the input sensitivity of any device.
- Input **1dB Compression Point** is a useful metric to describe the maximum input signal that will result in 1dB of gain compression in the signal chain.
- Input **Intercept Point** is a useful metric to describe the intermod distortion ratios generated for a given input signal level.
- **Selectivity** is a useful metric to describe the ability of a receiver to select a wanted signal and reject a nearby unwanted signal.
- **SFDR** (Spurious Free Dynamic Range) is a measure of the best case available instantaneous dynamic range.

A Quick Review of ADC Specifications

- **Full-Scale** is the maximum analog input voltage that will result in a maximum digital output signal level, usually expressed in units of Vp-p.
- **SNR** is the ratio of the RMS signal level to the RMS value of all other spectral components excluding DC and signal harmonics.
- **SINAD** is the ratio of the RMS signal level to the RMS value of all other spectral components including signal harmonics but excluding DC.
- **ENOB** is the effective number of bits presented by the ADC and is equal to (SINAD -1.76)/6.02 .



- Single-tone **SFDR** is a measure of the RMS signal level to the RMS level of the worst case peak spurious component (not necessarily harmonically related).



- Two-tone **SFDR** is a measure of the RMS signal level of either input tone to the RMS level of the worst case peak spurious component (not necessarily an intermod product).

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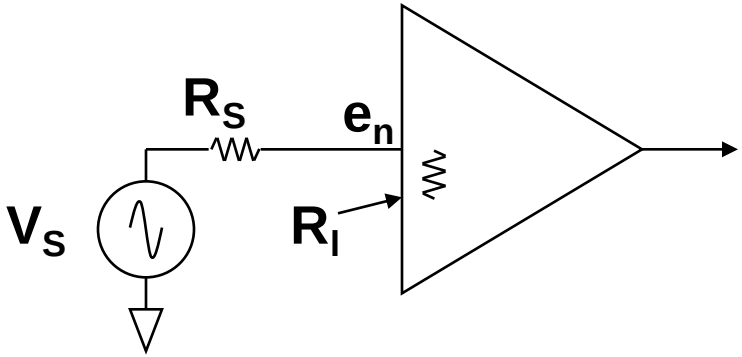
Translating Component Specifications to System Performance: nV/√Hz to NF



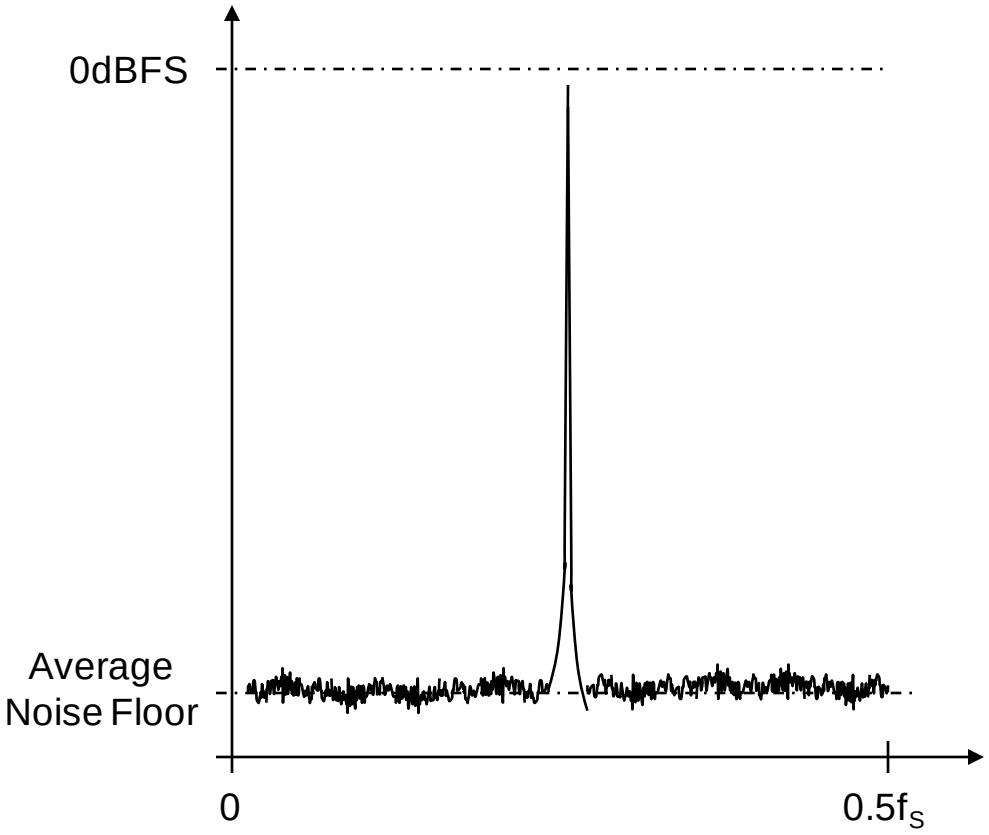
Converting input referred voltage noise density to NF

$$F = 1 + \frac{(e_n)^2}{4kTR_s\left(\frac{R_l}{R_l + R_s}\right)^2} \quad \& \quad NF = 10Log(F)$$

Example: Consider amplifier with 1nV/√Hz input referred noise density – 50Ω input impedance driven by a 50Ω source

$$F = 1 + \frac{(1nV/\sqrt{Hz})^2}{4\cdot(1.38\times10^{-23}\,Joules/K)\cdot(298K)(50\Omega)(\frac{1}{2})^2} = 2.216 \qquad \therefore NF = 10Log(2.216) = 3.5dB$$

Translating Component Specifications to System Performance: ADC SNR to NF



Effective noise density can be calculated by either:
1) computing the effective voltage noise density and convert to NF for a given impedance level
2) computing the full-scale power and calculate the effective noise power density and compare to kT.

$$\text{Effective Noise Power Density} = \text{FS (dBm)} - \text{SNR(dBFS)} - 10\text{Log}(0.5f_S)$$

- Effective Noise Power Density: dBm/Hz
- FS (dBm): Full-scale Power in dBm
- SNR(dBFS): SNR in dBFS
- $10\text{Log}(0.5f_S)$: Nyquist Zone In dBHz

Translating Component Specifications to System Performance: ADC SNR to NF

Example: ADC with 2Vp-p full-scale input is terminated to a 200Ω impedance level and the SNR is measured to be 72dBFS for a 200MHz sampling rate.

Calculation 1. 2Vp-p full-scale is an RMS level of 0.7071Vrms.

- Expressed in units of dBVrms as 20Log(0.7071Vrms) = -3.01dBVrms
- The wideband noise floor is 72 dB below Full-Scale, at -75.01dBVrms
- The sampling rate is 200MHz, so the Nyquist zone is 100MHz, or 80dBHz
- Therefore the noise density is -75.01dBVrms – 80dBHz = -155dBVrms/Hz
- Converted to linear units as $10^{(-155/20)}$ = 18nV/√Hz.
- Using the nV/√Hz to NF equation for a 200Ω reveals a NF of 26 dB

Calculation 2. 2Vp-p full-scale is an RMS level of 0.7071Vrms.

- Into a 200Ω impedance level this is a full-scale power of 4 dBm
- The wideband noise floor is 72 dB below Full-Scale, at -68dBm
- Over 80dBHz, an average power density of -68dBm – 80dBHz = -148dBm/Hz
- -148dBm/Hz is 26dB above kT (-174dBm/Hz), ∴NF is again found to be 26dB.

High-IF Sampling ADC Drivers

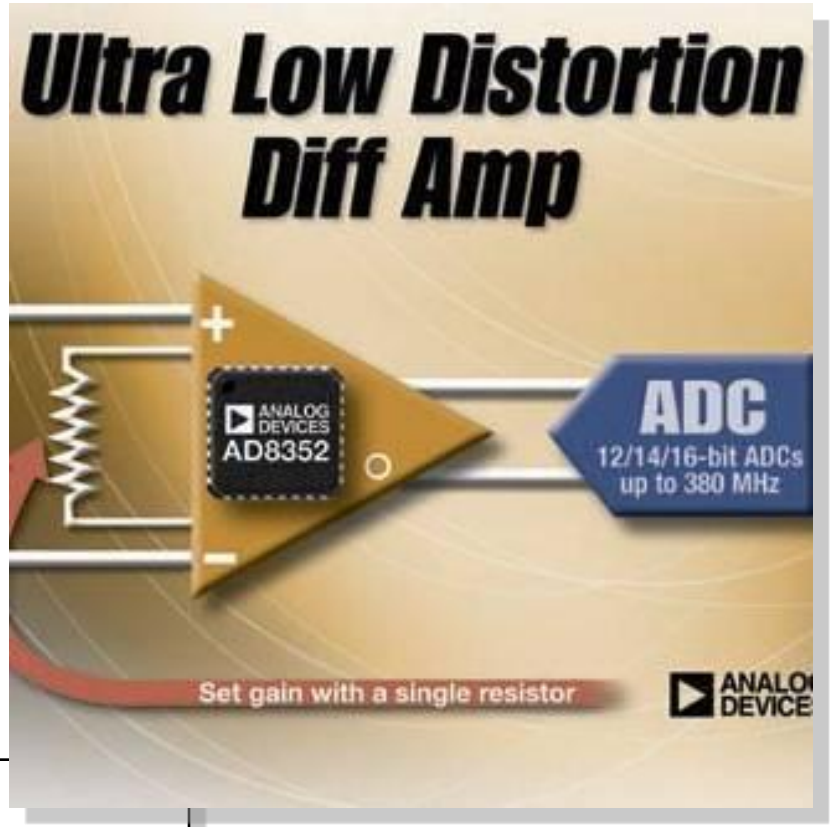
Part No.	Useful BW (MHz)	Gain (dB) Control	OIP3 (dBm)	Noise Figure (dB)	Supply	Package
ADA4937	100	0 to 18 resistive	37 @ 70MHz	15	5V@ 38mA	3x3mm 16-LFCSP
AD8352	**350**	**3 to 28 resistive**	**41 @ 140MHz**	**15.5**	**5V@ 37mA**	**3x3mm 16-LFCSP**
ADL5530	1000	17 fixed	37 @ 190MHz	3	5V@ 110mA	3x2mm 8-LFCSP
AD8368	380	-12 to 22 analog	34 @ 70MHz	9.5	5V@ 60mA	4x4mm 24-LFCSP
AD8370	200	-25 to 34 digital	35 @ 70MHz	7	5V@ 79mA	16 – lead TSSOP
AD8375/6	**500**	**-4 to 20 digital**	**50 @ 200MHz**	**8**	**5V@ 125mA**	**4x4mm 24-LFCSP**

AD8352 Lowest Distortion Differential Amplifier

Highest Performance Differential ADC Driver on the Market

KEY SPECIFICATIONS

- Wide 3 dB Bandwidth: 2 GHz
- Low Distortion
  - 10 MHz: −86 dBc HD2, −82 dBc HD3
  - 70 MHz: −84 dBc HD2, −82 dBc HD3
  - 190 MHz: −81 dBc HD2, −87 dBc HD3
- High Linearity: OIP3 41dBm @ 150 MHz
- Low Input Noise: 2.6 nV/√Hz @ 10 dB Gain
- Package: 3mm×3mm 16-lead LFCSP



FEATURES

- Single Resistor Sets Gain 3 dB to 25 dB
- Single Resistor and Capacitor Distortion Adjustment

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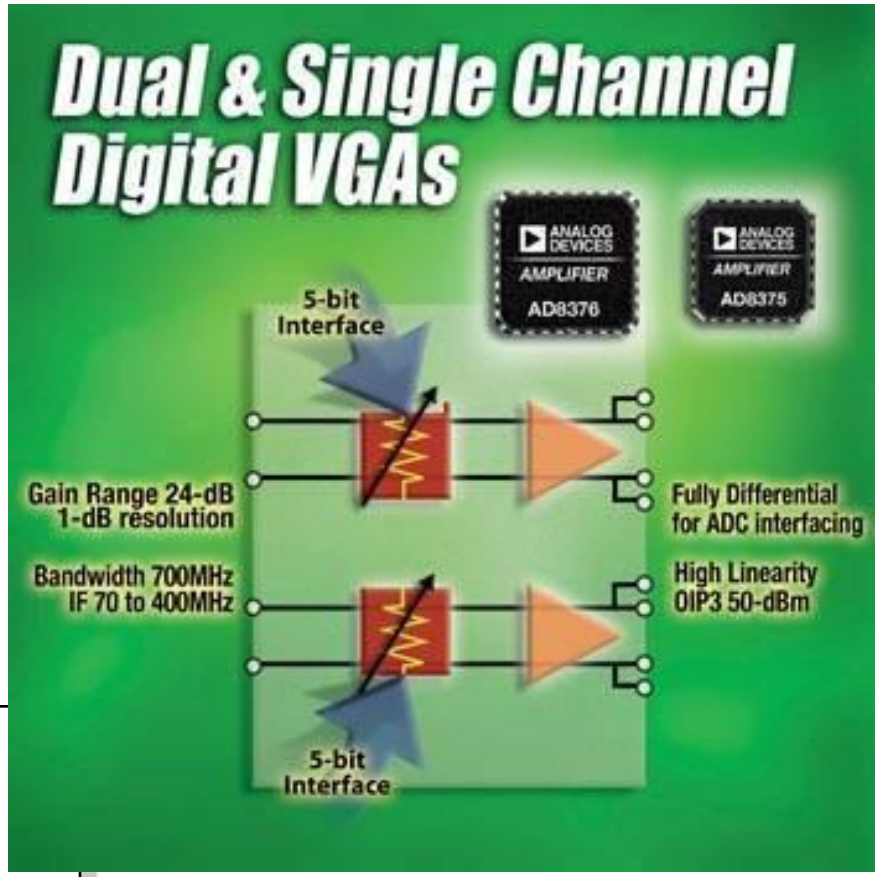
AD8375/6 Single/Dual Programmable DGA

KEY SPECIFICATIONS

- 3 dB Bandwidth: 700 MHz
- OIP3: 50 dBm @ 200 MHz
- 2nd/3rd Harmonic: -85/-92 dBc @ 200 MHz
- Noise Figure: 8.3 dB @ 190 MHz
- Differential Input/Output
- Gain Control Range: -4 dB - 20 dB
- AD8375 Package: 4mm×4mm 24-LFCSP
- AD8376 Package: 5mm×5mm 32-LFCSP

FEATURES

- Digitally-Controlled Amplifier/Attenuator
- Optimized for Driving IF Sampling ADCs
- Differential or Single-Ended Input Drive
- Fully-Balanced Differential Signal Path
- 1 dB Gain Step Size



AD8376 Dual of AD8375

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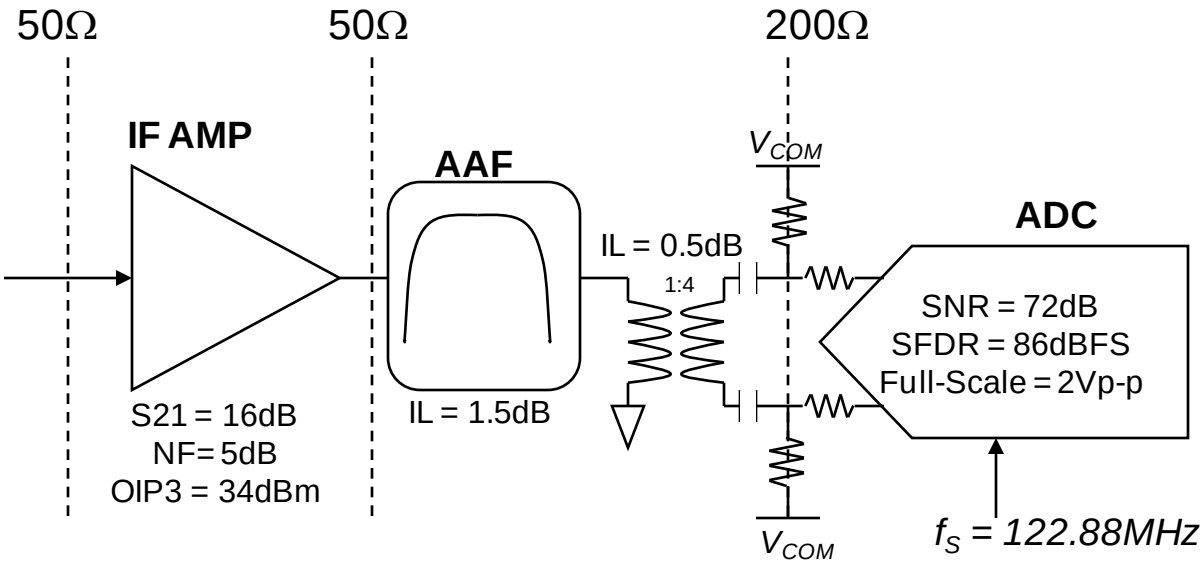
Amplifier and ADC modeling

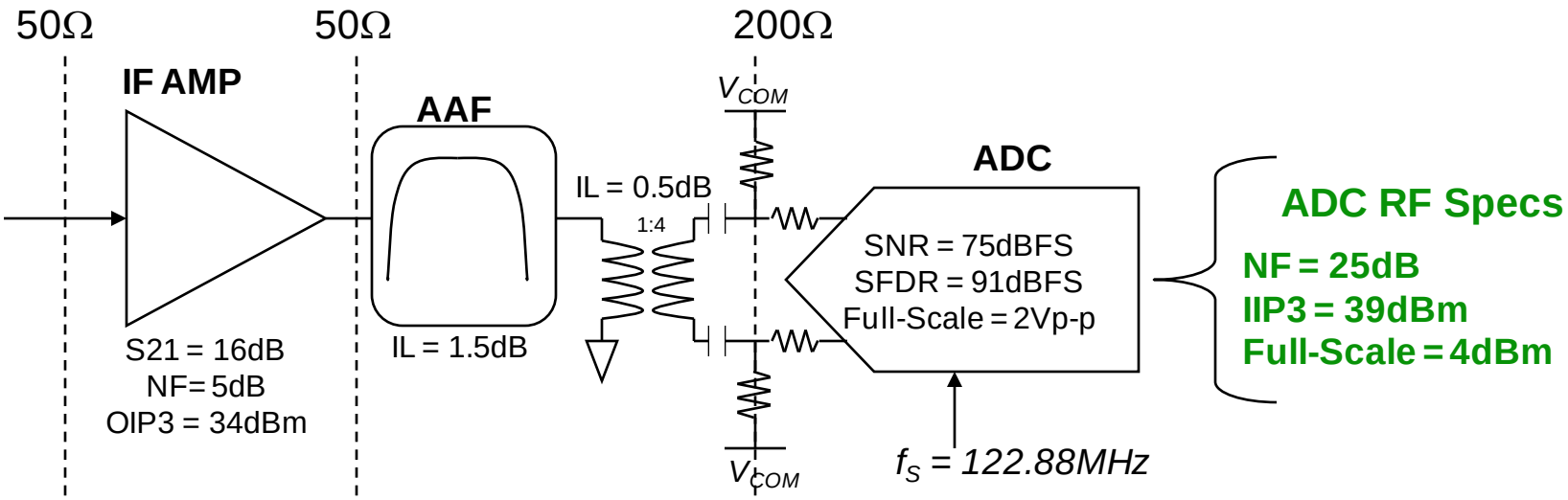
- It's important to consider the cascaded performance before committing to hardware
- This requires careful inspection of component performance, usually derived from datasheet data
- Often necessary to transform specifications so they are depicted using a common set of units (dBm or dBVrms, dBm/Hz or nV/√Hz)
- Need to be cautious about impedance levels and matching/interface networks
- The proceeding examples are designed to help extract data and model system performance before committing to hardware

Single-Ended Input Interface Example



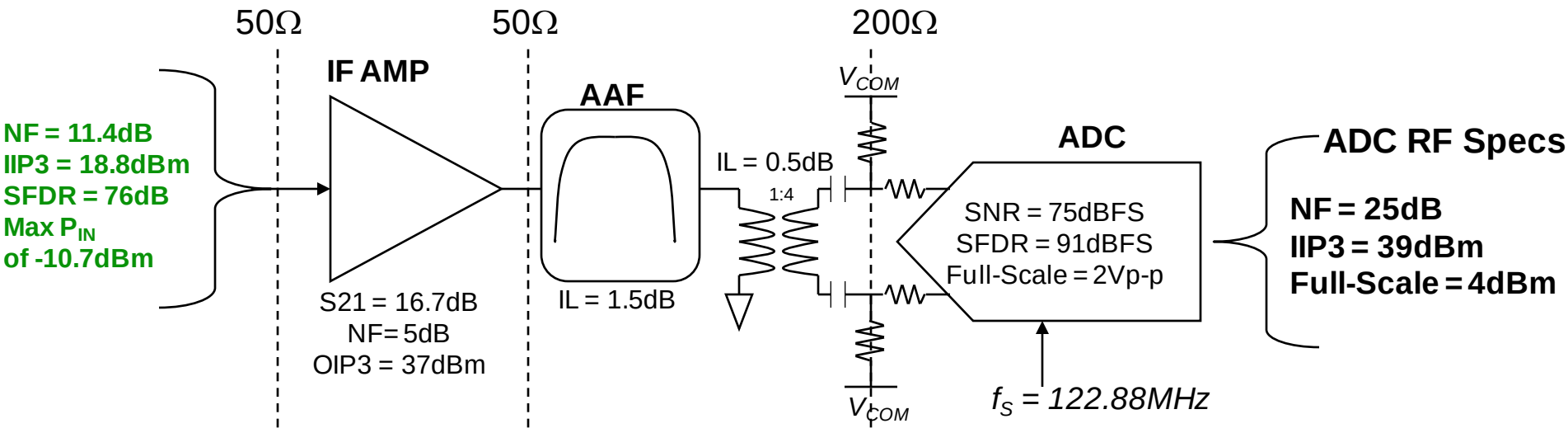
- In this example we assume the ADC is terminated to present 200Ω and a 1:4 impedance ratio transformer is used to match to a 50Ω anti-aliasing filter.
- For help with ADC matching see AN-935 and AN-827.

Single-Ended Input Interface Example



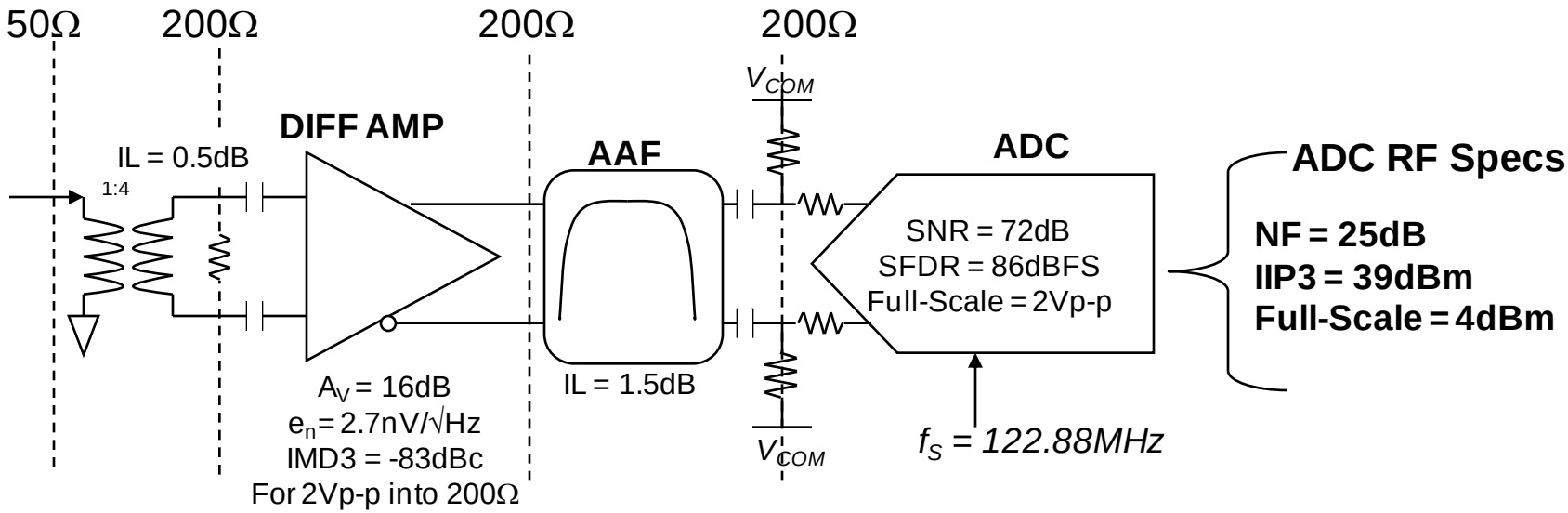
- **Next we need to transform component specifications so they share a common set of units (intercepts in dBm or dBVrms, noise in terms of dBm/Hz or nV/√Hz)**
- **The ADC specs usually require the most attention. (see AN-835 for help)**
  - Full-Scale of 2Vp-p terminated into 200Ω is a full-scale power level of 10Log((2/2√2)2/200) = -26dB or **4dBm**.
  - SNR of 75dBFS indicates that the wideband noise floor is 75dB below full-scale or at (4dBm-75dBFS) = -71dBm.
    Integrated over the full Nyquist zone of 61.44MHz, therefore the input power density must be -71dBm – 10Log(61.44MHz) = -149dBm/Hz. That's a NF of **25dB**.
  - The 91dBFS two-tone SFDR spec means that the |IMD3| would be 84dBc for two tones set at -7dBFS. That's an IIP3 of ((4dBm-7dBFS)+84dBc/2) = **39dBm**.

Single-Ended Input Interface Example



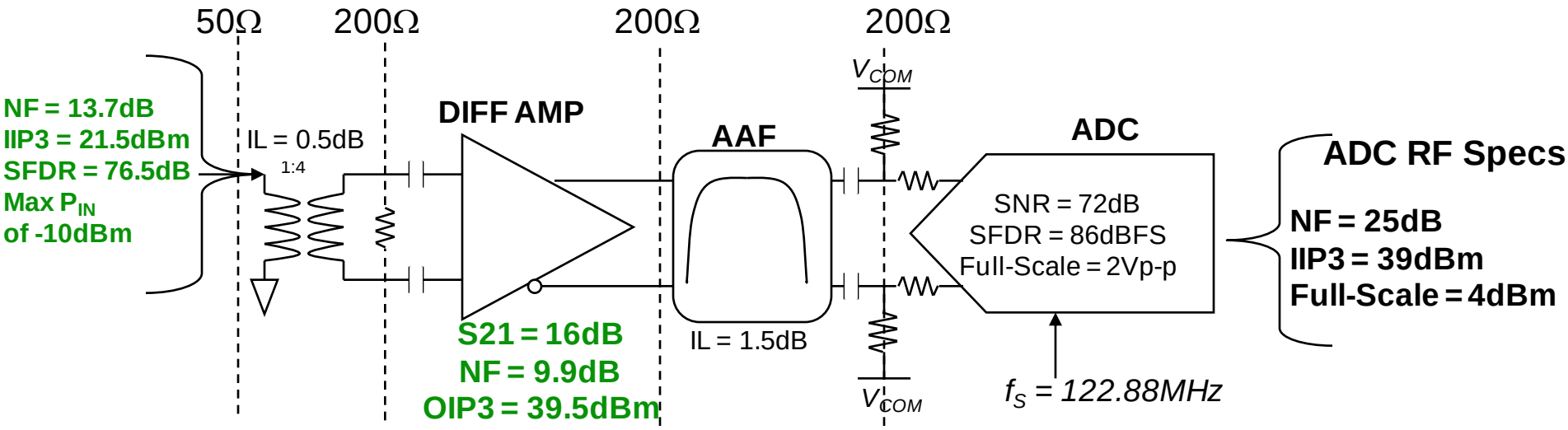
Spec	IF AMP	AAF	XFMR	ADC
NF - dB	5	1.5	0.5	25
S21 - dB	16.7	-1.5	-0.5	0
IIP3 - dBm	20.3	100	100	39
OIP3 - dBm	37	98.5	99.5	39

Differential Interface Example



- **Start with identifying target impedance levels and defining the ADC RF specs.**
- **It may be necessary to transform diff-amp specs**
  - **For the example, a 2.7nV/√Hz input density terminated to match a 200Ω source is a NF of 10Log(1 + (2.7nV/√Hz)²/((4kT200Ω)(1/2)²)) = 9.9dB.**
  - **The IMD3 is -83dBc into a 200-Ohm load for a 2Vp-p composite output. A two tone signal of 2Vp-p means each tone is at 1Vp-p. Into 200-Ohms this is a single-tone power level of -2dBm per tone. Therefore the OIP3 is -2dBm + 83 / 2 = 39.5dBm**

Differential Interface Example



Spec	XFMR	DIFF AMP	AAF	ADC
NF - dB	0.5	9.9	1.5	25
S21 - dB	-0.5	16	-1.5	0
IIP3 - dBm	100	23.5	100	39
OIP3 - dBm	99.5	39.5	98.5	39

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Passive Transformer Coupled vs Active

"Passive" Transformer

Spec	IF AMP	AAF	XFMR	ADC	Total
NF - dB	5	1.5	0.5	25	11.4
S21 - dB	16.7	-1.5	-0.5	0	14.7
IIP3 - dBm	20.3	100	100	39	18.8
OIP3 - dBm	37	98.5	99.5	39	33.5

SFDR = 76dB

Max P_{IN} = -10.7dBm

Would be Max P_{IN} = 6dBm w/o amp

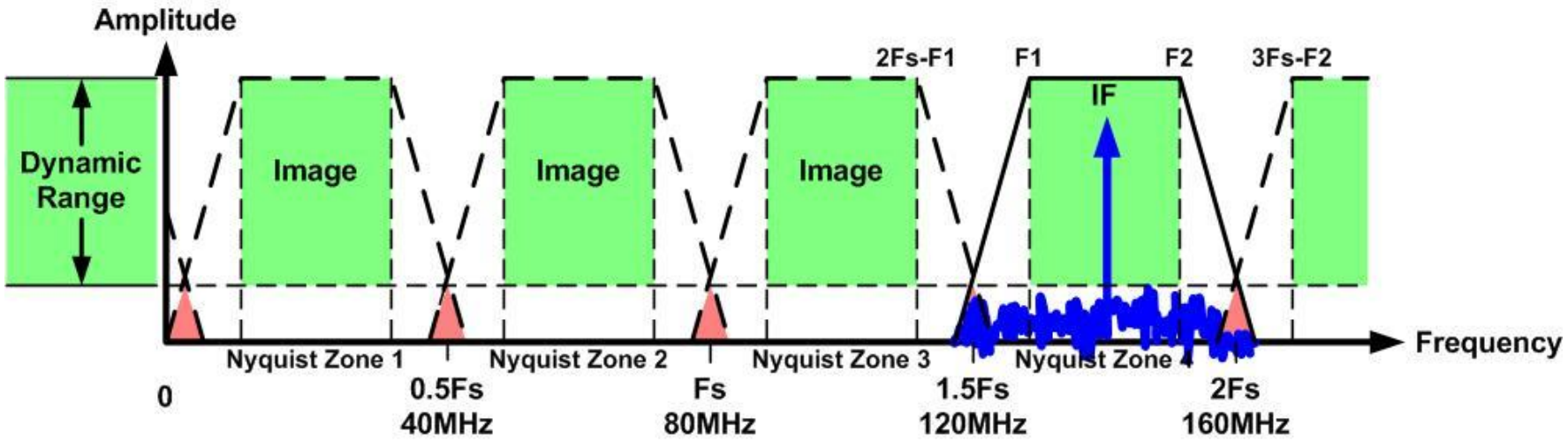
Active Interface

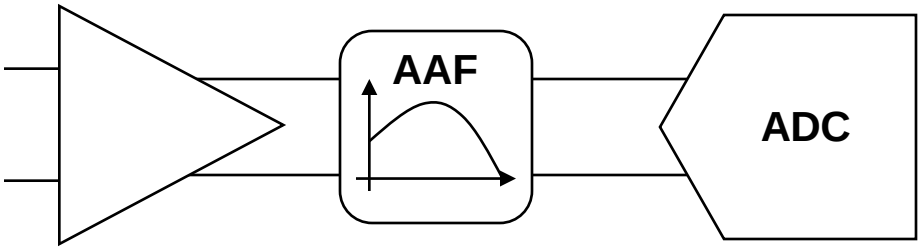
Spec	XFMR	DIFF AMP	AAF	ADC	Total
NF - dB	0.5	9.9	1.5	25	13.7
S21 - dB	-0.5	16	-1.5	0	14.0
IIP3 - dBm	100	23.5	100	39	21.5
OIP3 - dBm	99.5	39.5	98.5	39	35.5

SFDR = 76.5dB

Max P_{IN} = -10dBm

Why use an Anti-Aliasing Filter???





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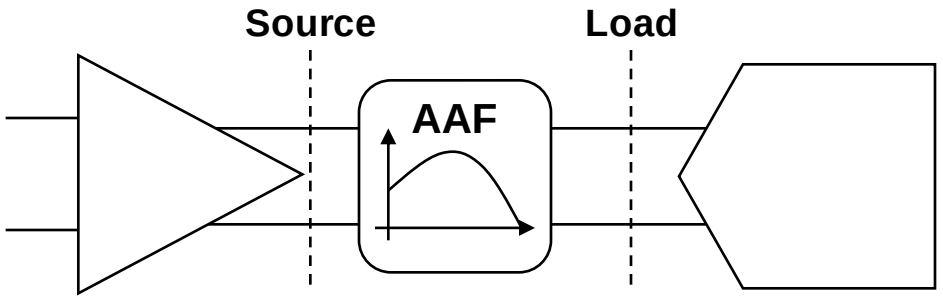
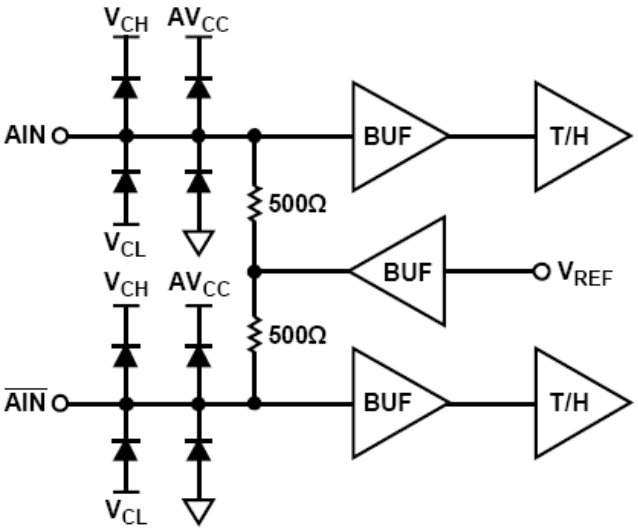
Filter Designs Considerations

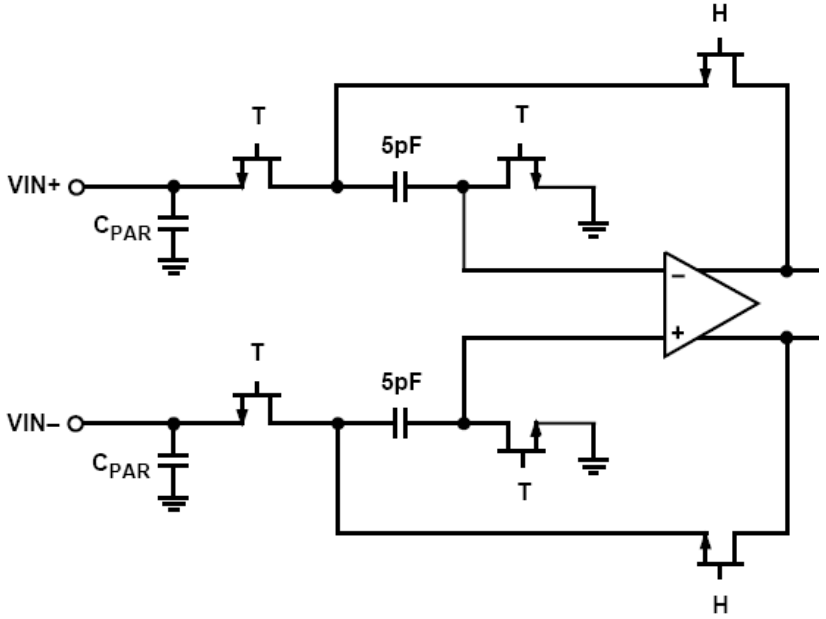
- Determine Cut-Off, Roll-Off, Ripple and Group Delay
- Select Filter Topology



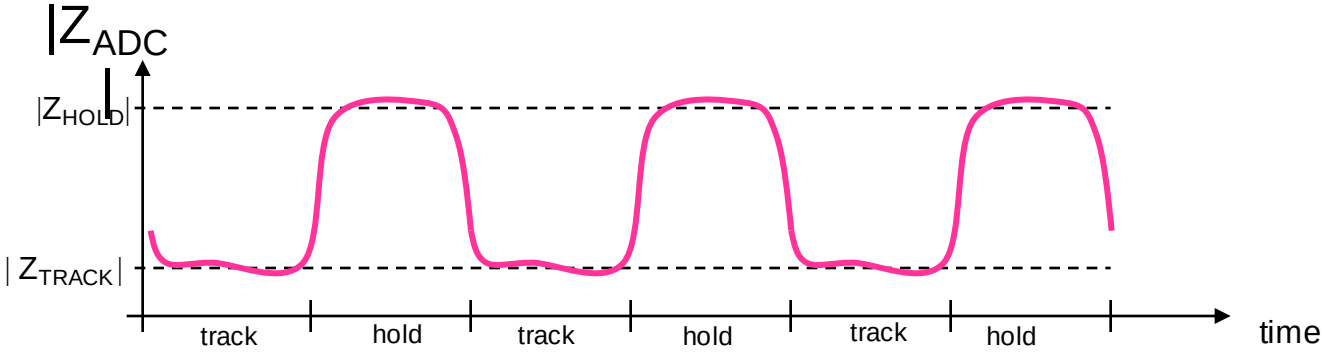
- Switching capacitor
  - Resonant match
- Impedance match
  - AD8352
    - Load with 200 Ohms
    - Presents 100 Ohms source impedance
  - AD8375
    - Load with 150 Ohms
    - Open collector output requires biasing
    - Presents high impedance output

Working with ADC Input structures





Raw Track and Hold ADC Front End



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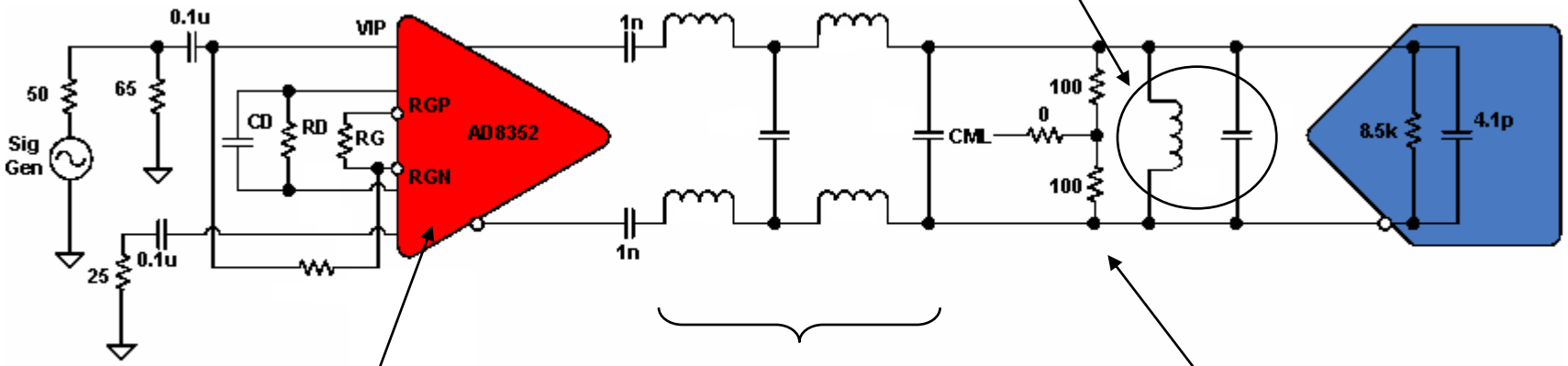
AD8352 Design Example



Resonant Match using Shunt L
(get rid of ADC raw switched cap)

4th Order Filter
(100Ω AD8352 output
to 200Ω Load)

Using the AD8352 as the
Single-Ended to Differential

Suggested Bias Network
and Reactive Match at
ADC input
(presents 200Ω Load)

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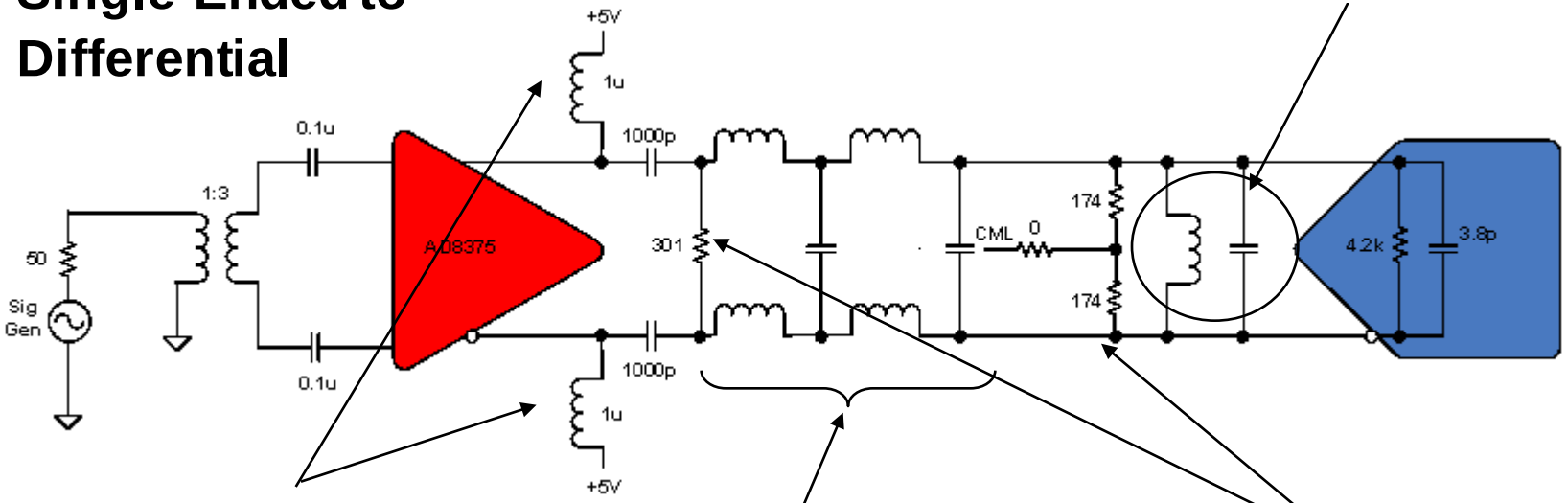
AD8375 Design Example

Using transformer as Single-Ended to Differential

Resonant Match using Shunt L (get rid of ADC raw switch cap)



Choke Inductors (High Z output)

4th Order Filter (300Ω at AD8375 output to 300Ω filter output)

Suggested Bias Network and Reactive Match at ADC input (split up, but still presents a 150Ω Load)

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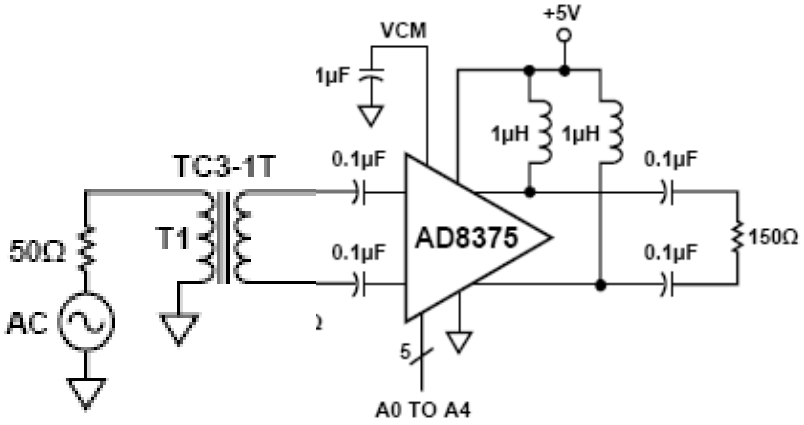
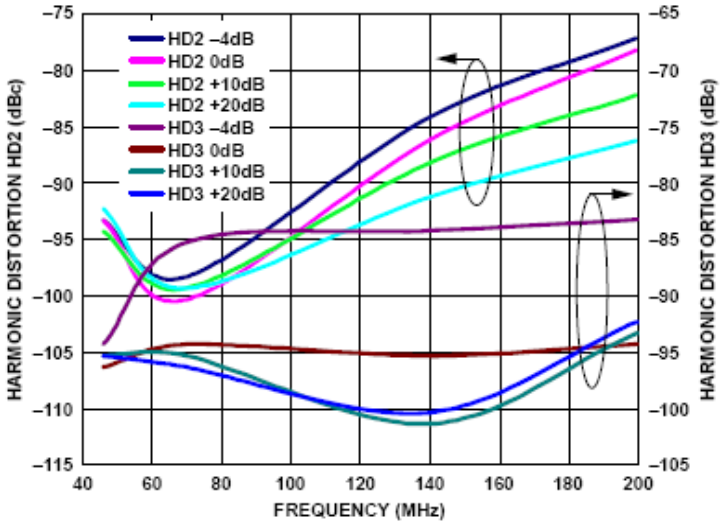
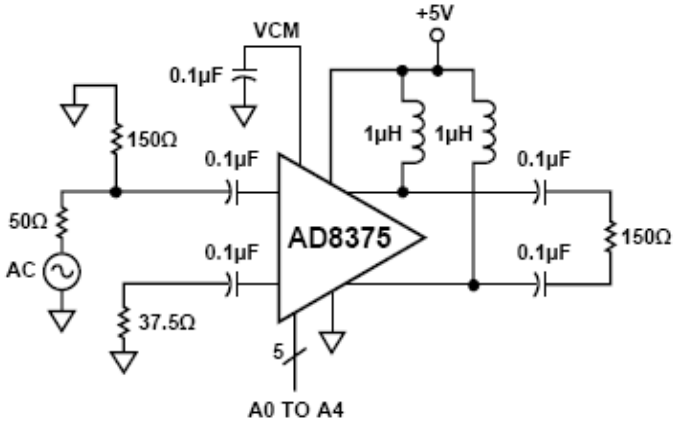
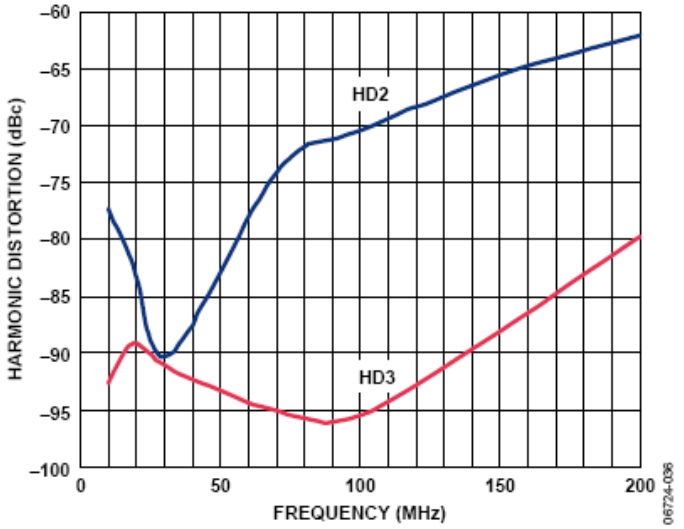
Most Commonly Encountered Issues

- **Single-Ended Driving – NO BALUN?**









decreases power gain by 3 dB & limits distortion cancellation

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AD8375/76 & AD6655 IF Receive Design Example: Requirements

Narrowband IF Receive (Resonant) Match

System Requirements

Sample Rate = 122.88MSPS
SNR = ≥71dB = 14bits
Input Frequency = 153.6MHz
Band = 15MHz (146.1-161.1MHz)

→ AD8375 & AD6655, 14-bit, 125MSPS, 1.8V, Diversity Receiver

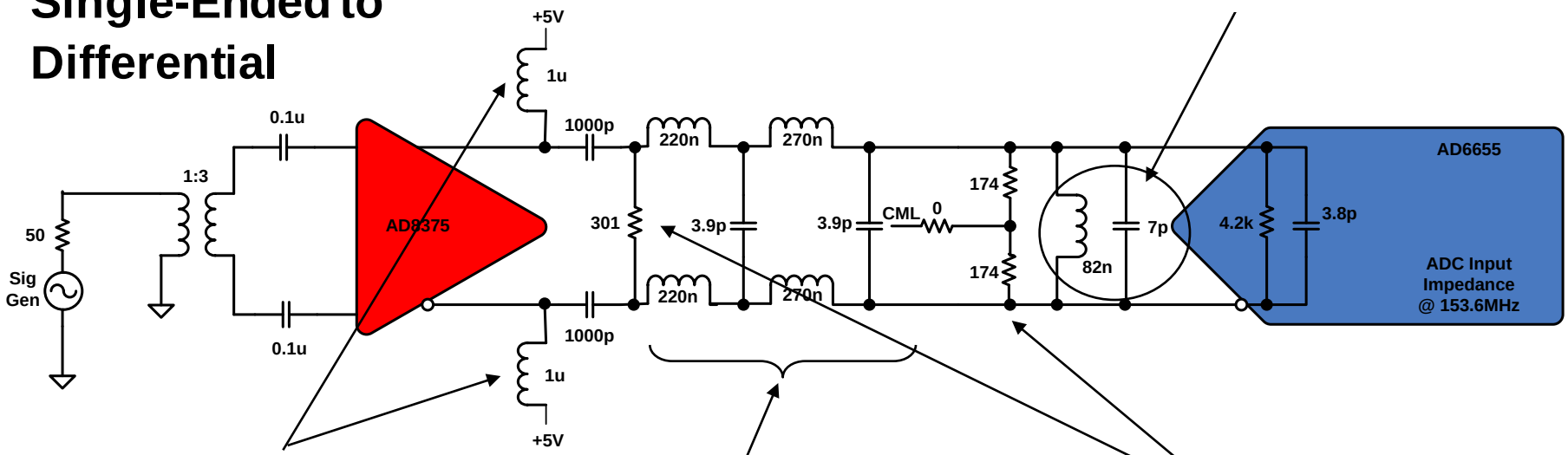
Design Requirements

Boundaries	Input Impedance (Ohm)	VSWR	Passband Flatness (dB)	IF -3dB BW (MHz)	SNR (dBc)	SFDR (dBc)	Input Drive Level (dBm)
Ideal Value	50	1	<0.5	170	71	85	NA
Design Limit	30	1.5	<1	200	70	80	NA

AD8375 & AD6655 Design Example: Final Schematic Diagram

Using transformer as Single-Ended to Differential

Resonant Match using Shunt L (get rid of ADC raw switch cap)



Choke Inductors (High Z output)

4th Order Filter (300Ω at AD8375 output to 300Ω filter output)

Suggested Bias Network and Reactive Match at ADC input (split up, but still presents a 150Ω Load)

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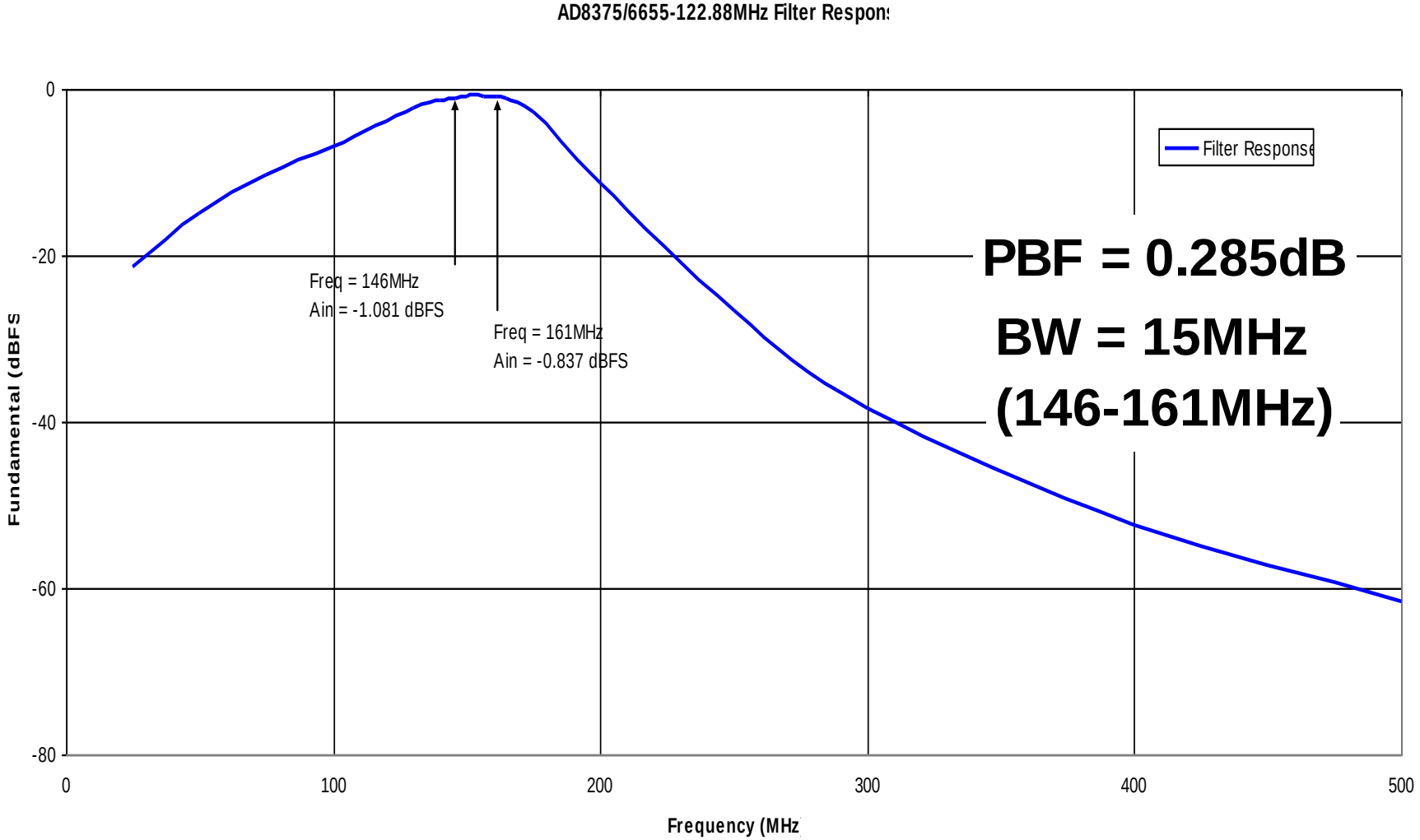
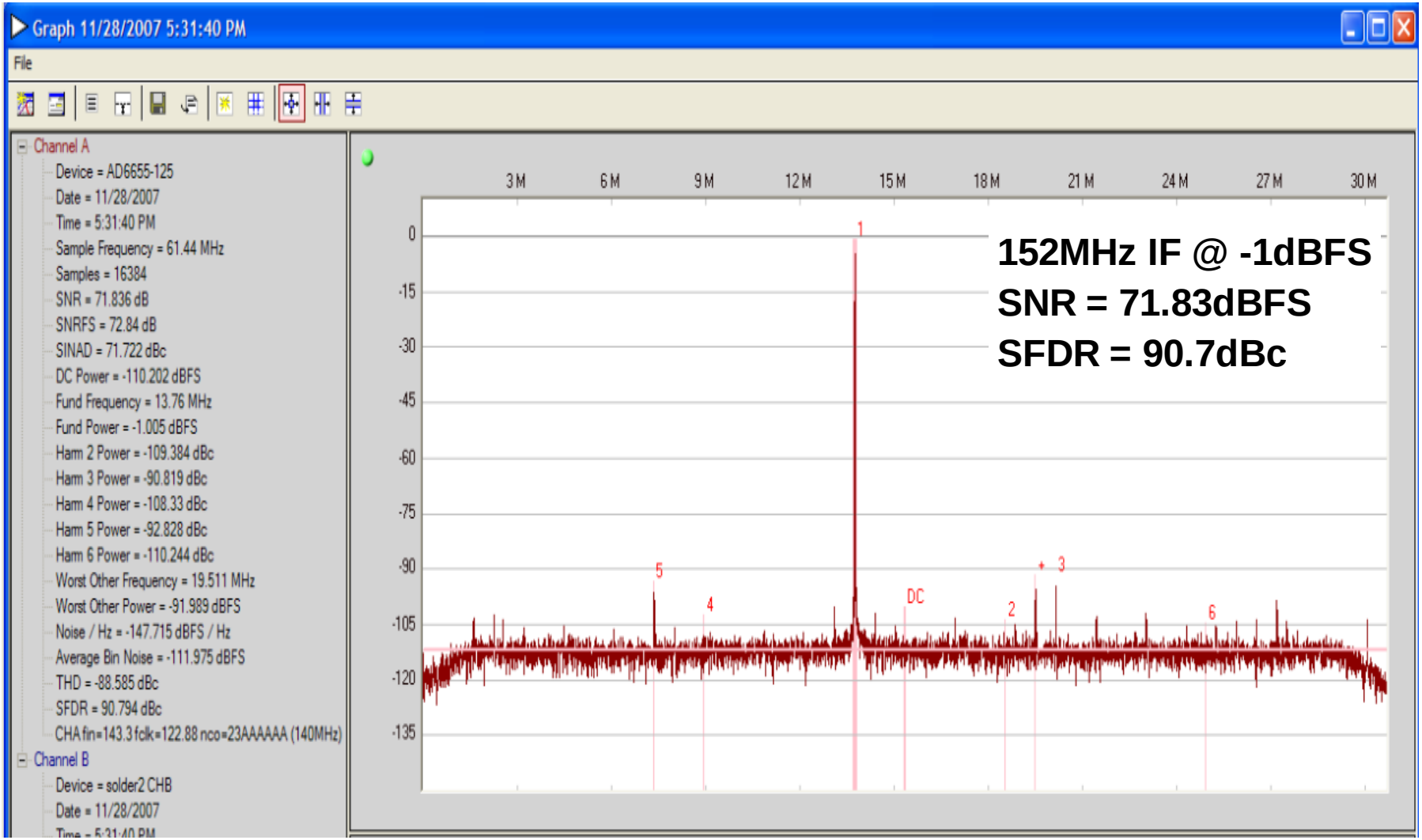
AD8375 & AD6655 Design Example: BW, Passband Flatness, Input Drive



AD8375 & AD6655 Design Example: FFT Performance



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Further Reading:

- **Application Notes**
  - AN-742, Frequency Domain Response of Switched-Capacitor ADCs
  - AN-827, A Resonant Approach to Interfacing Amplifiers to Switch-Capacitor ADCs
  - AN-835, Understanding High Speed ADC Testing and Evaluation
  - AN-935, Designing an ADC Transformer-Coupled Front End
- **S-parameter data**
  - AD9215/26/35/36/37/44/45 webpage, click on Evaluation Boards, upload S-parameter data in an MSExcel spreadsheet
- **Papers**
  - Transformer-Coupled Front-End for Wideband A/D Converters – April Issue Analog Dialogue 2005
  - Pushing the State of the Art with Multichannel A/D Converters – May Issue Analog Dialogue 2005
  - Which ADC Architecture is Right for Your Application – June Issue Analog Dialogue 2005
  - Wideband A/D Converter Front-End Design Considerations – When to Use a Double Transformer Configuration– July Issue Analog Dialogue 2006
  - Wideband A/D Converter Front-End Design Considerations II - Amplifier- or Transformer Drive for the ADC? – February Issue Analog Dialogue 2007
- **Datasheets**
  - AD9233/46, 80MSPS 12/14bit, 1.8V, Switched-Capacitor ADC
  - AD9445/46, 80MSPS 14/16bit, 5/3V, Buffered ADC
  - ADA4937
  - AD8352
  - AD8375/76

Thank-you!

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