



APPLICATION NOTE 2032

Trimless IF VCO: Part 1: Design Considerations

Abstract: This application note explores the design fundamentals needed to implement a trimless, fixed-frequency, IF voltage-controlled oscillator (VCO) and points out the challenges in guaranteeing proper circuit operation. VCOs are essential components in the architecture of most wireless systems. In dual-conversion approaches, a fixed-frequency IF VCO is required to control the frequency translation from IF to baseband and/or baseband to IF.

Additional Information: [Trimless IF VCO: Part 2: New ICs Simplify Implementation](#)

Part 1 of this two-part article explores the design fundamentals needed to implement a trimless, fixed-frequency, IF voltage-controlled oscillator (VCO) and points out the challenges in guaranteeing proper circuit operation. VCOs are essential components in the architecture of most wireless systems. In dual-conversion approaches, a fixed-frequency IF VCO is required to control the frequency translation from IF to baseband and/or baseband to IF.

Dual-conversion systems require two oscillators. Typically, the first (RF VCO) tunes over the full range of input channel frequencies, and the second (IF VCO) operates at a single frequency established by the frequency plan. The RF VCO is available as a module, IC, or discrete-component circuit, with modules and ICs being more common. For IF VCOs, small, cost-effective modules are nearly absent from the market. Probable reasons include the need for many arbitrary IF frequencies and the need for large-valued inductors that cannot be laser-trimmed (adjusted) in production. As a result, the IF VCO is usually implemented as a discrete circuit or as part of an IC.

Maxim has pioneered a new VCO IC intended for use in wireless systems whose other board-level RF/IF ICs lack that function. Part 2 of this article will introduce the IC, discuss its development, and detail the simple and cost-effective applications it makes possible.

A discrete-component VCO offers sufficient degrees of freedom to meet the performance objectives of most systems (tuning range, output power, phase noise, current consumption, cost, etc.). For higher volume, cost-sensitive modern products, however, production-line adjustment of the oscillation frequency is not acceptable. The RF engineer is therefore compelled to devise a VCO that requires no adjustments during assembly, i.e., a trimless VCO. The design is not trivial. In addition to an understanding of VCO design fundamentals, it requires substantial RF engineering effort to ensure that the design is properly centered and that the oscillator tunes to the desired frequency over all allowed variations in component values, temperature, and supply voltage. The following discussion, while explaining pertinent issues in the design of a trimless IF VCO, seeks to develop an appreciation for the magnitude of the task.

VCO Topology

While several oscillator topologies are viable for construction of a practical RF VCO, the one that has proven successful in many commercial VCO modules and countless discrete VCO circuits is the Colpitts common-collector topology (**Figure 1**). This topology is useful for a wide range of operating frequencies, from IF to RF.

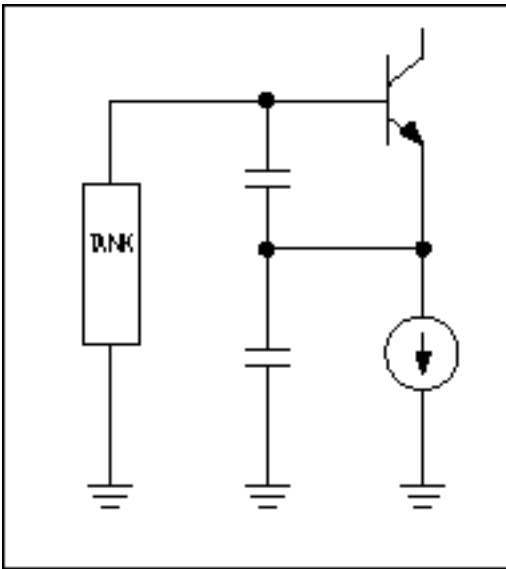


Figure 1. The basic Colpitts oscillator.

A flexible, low-cost, and reasonably high-performance VCO may be constructed with an inductor-capacitor (LC) tank circuit consisting of a low-cost surface-mount inductor and varactor diode. The oscillator tank is a parallel-resonant circuit controlling the oscillation frequency; any change in the inductor or capacitor changes the oscillation frequency. The inductor and varactor can implement the variable resonance as a parallel- or series-mode network.

The parallel-mode network may be used at lower frequencies where large-value varactors are impractical and the inductor value can be made larger. The parallel-mode configuration also permits a straightforward analysis of the oscillator. For the remainder of this article, the trimless IF VCO will be illustrated with a Colpitts-style oscillator, using a parallel-mode LC tank (**Figure 2**).

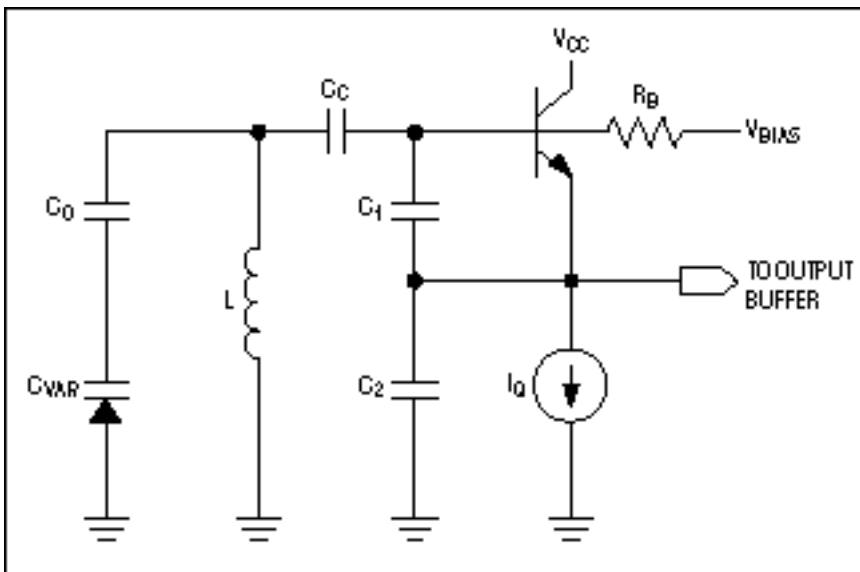


Figure 2. Use of the Colpitts topology in a VCO.

The Colpitts oscillator is discussed in several textbooks (Clarke and Hess 1978, Hayward 1994, Rohde 1998), and various equations have been derived to predict the behavior of oscillators in general and the Colpitts topology in particular. The oscillator is generalized with a feedback-amplifier model of the circuit. Expressions for the exact oscillation frequency may be derived by equating impedances in that model, but those expressions are cumbersome and provide little insight into the design process.

Alternatively, the Colpitts oscillator can be analyzed in a simpler but less accurate manner, which provides a set of design equations that are clearer, more insightful, and useful for first-order oscillator design. First, the Colpitts oscillator may be redrawn as an LC amplifier with positive feedback (**Figure 3**). This view is useful in calculating the loop gain, oscillation amplitude, and phase noise. To predict startup behavior and oscillation frequency, the original circuit can also be redrawn as a negative impedance plus resonator structure (**Figure 4**). Equations from

these two views are combined as a set of governing equations for the Colpitts oscillator (Meyer 1998).

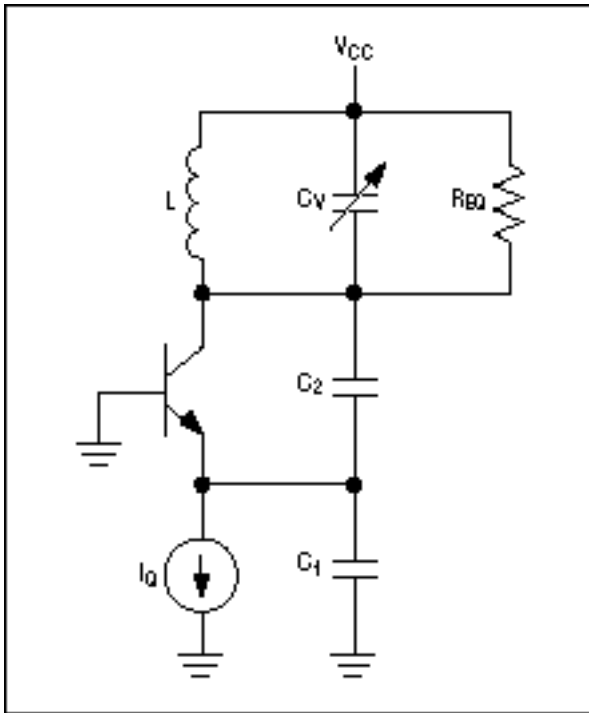


Figure 3. LC amplifier model.

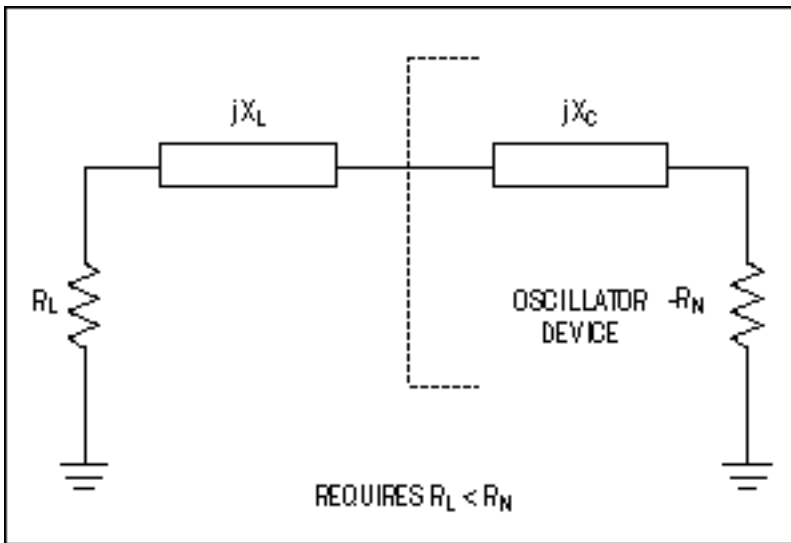


Figure 4. Reflection amplifier model.

Basic Design Equations for the Colpitts Oscillator

Ignoring parasitic elements, the basic equations for this analysis assume that $C_C > C_1$ and C_2 , and $C_1 > C_\pi$ (C_π is the base-emitter capacitance). Calculate the oscillation frequency (f_O) as follows:

$$f_O = \frac{1}{2\pi\sqrt{L \times C_T}}, \quad C_T = C_V + C_{12},$$

$$C_V = \frac{C_{VAR} \times C_O}{C_{VAR} + C_O}, \quad C_{12} = \frac{C_1 \times C_2}{C_1 + C_2} \quad (1)$$

Calculate the quality factor of the resonant tank circuit (Q_T) as follows:

$$Q_V = \frac{1}{2\pi \times C_V \times R_S \times f_O}, \quad R_{QC} = Q_V^2 \times R_S, \quad (2)$$

$$Q_T = \frac{R_{EQ}}{2\pi \times L \times f_O}, \quad R_{EQ} = R_{QL} \parallel R_{QC}$$

Estimate the oscillation amplitude as follows:

$$V_O \cong 2 \times I_Q \times R_{EQ} \times \frac{J_1(\beta)}{J_0(\beta)}, \quad (3)$$

$$V_O \cong I_Q \times R_{EQ} \times 1.4$$

Calculate the loop gain and startup criteria as follows:

$$\text{Loop gain} = g_m \times R_{EQ} \times \frac{1}{n}, \quad \text{where } n = \frac{C_1 + C_2}{C_2} \quad (4)$$

Startup criteria:

$$\frac{g_m}{(2\pi \times f_O \times C_1)(2\pi \times f_O \times C_2)} \gg \frac{R_{EQ}}{Q_T^2}, \quad (5)$$

minimum 2:1 ratio

Calculate the Colpitts oscillator phase noise (PN) at an offset frequency (f_m) from the carrier as follows:

$$\text{PN} = i_n^2 \times \frac{1}{V_O^2} \times \left(\frac{f_O}{2Q_O} \right)^2 \times \frac{R_{EQ}^2}{f_m} \quad (6)$$

Trimless VCO Approach

Developing a trimless VCO is relatively simple in concept. Oscillator-frequency adjustments can be eliminated if the oscillator has sufficient extra tuning range to overcome all the error sources (e.g., component tolerances) that produce shifts in frequency. At first glance, it may seem intuitive and simple enough just to provide plenty of oscillator tuning range and tune out all the error sources. For a given tuning-voltage range, however, finite variable capacitance imposes a fundamental limit on the frequency-tuning range, and the VCO's electrical-performance requirements often constrain the tuning range before that limit is reached.

Unfortunately, several negative consequences attend an oscillator with excessive tuning range. Very wide ranges require heavy capacitive coupling of the varactor to the tank, which substantially reduces the tank-circuit Q. The result is greater phase noise (reduced tank amplitude vs. transistor noise), greater sensitivity to tuning-line noise (which translates directly into frequency modulation), the possibility of too much voltage swing across the varactor, potential startup problems, and greater challenge in designing the loop filter. These factors lead to the conclusion that excessive tuning range is undesirable. Indeed, it should be no greater than the minimum necessary to absorb all error sources.

Glossary
C_O = varactor coupling capacitance
C_T = total tank capacitance
C_{VAR} = varactor capacitance
f_m = offset frequency of PN in Hz
f_O = frequency of oscillation
g_m = bipolar transistor (oscillator) transconductance
i_n = collector shot noise
I_Q = oscillator transistor bias current
Q_L = inductor Q
Q_T = tank Q
Q_V = effective varactor Q
R_{EQ} = equivalent tank parallel resistance
R_S = varactor series resistance
V_O = RMS tank voltage

A wider tuning range causes greater oscillator phase noise through two well-understood phenomena: a reduction in the tank-circuit Q and noise on the tuning line. To achieve a wider tuning range, the varactor must be coupled more heavily into the tank circuit. This coupling reduces the Q of C_V (the effective variable capacitance) as shown in Equation 2. Lower Q for C_V reduces the net Q of the tank and, consequently, increases the phase noise, per Equation 6.

The second factor in reducing phase noise is thermal noise on the tuning input, which creates FM-sideband noise. This noise increases with tuning range, and it can exceed the oscillator's inherent phase noise. The phase noise induced by thermal noise is given by:

$$PN = 20 \log \left(\frac{\sqrt{2} \times K_V \times V_n}{2 \times f_m} \right), \text{ where } K_V =$$

$$\text{VCO gain in } \frac{\text{Hz}}{\text{V}}, V_n = \text{noise density} \quad (7)$$

$$\text{at } V_{TUNE} \text{ input at } f_m \text{ in } \frac{\text{V}}{\sqrt{\text{Hz}}}$$

It is evident in both cases that phase noise degrades with increasing tuning range. To preserve low phase noise in a trimless VCO, therefore, it is critically important to provide *just enough* tuning range to meet the guaranteed bandwidth and accommodate the expected error sources.

As the varactor is coupled-in more heavily, more tank-voltage swing appears across the varactor, and the varactor voltage swing must be limited to avoid forward-biasing the varactor. This sets a limit on signal power in the tank and, consequently, on the oscillator's phase noise. Finally, startup problems may occur if the tank-

circuit equivalent series resistance (ESR) becomes too high (refer to the equations). A VCO with very wide frequency-tuning range may not start up properly, especially over the extremes of temperature. With the goal of providing just enough tuning range, the question is-how much?

Error Sources in the Oscillation Frequency

The trimless VCO's frequency tuning range is increased to accommodate error sources in the oscillation frequency. These error sources fall in two categories: error in the component values and error from design centering. The LC components that set the oscillation frequency are not ideal, of course. They contribute the following:

- Part-to-part variations (tolerance)
- Non-ideal performance (limited frequency response due to inductance, capacitance, and series resistance in the leads)
- Error induced by parasitic capacitance and inductance in the circuit layout

On the other hand, design-centering errors result from uncertainty in centering the VCO tuning range during the design process.

Component-Tolerance Error

Each capacitive and inductive component affecting the oscillation frequency in an LC oscillator has only limited part-to-part accuracy, and this tolerance error contributes to error in the oscillation frequency. **Table 1** lists the typical tolerances for the frequency-setting components in the oscillator.

Table 1. Oscillator frequency-setting component tolerances

Component	Tolerance
Varactor	$\pm 15\%$ at $V_{TUNE} = 0.4V$, $\pm 10\%$ at $V_{TUNE} = 2.4V$
Inductor	$\pm 5\%$
Capacitors	$\pm 5\%$
Parasitic Capacitance	$\pm 10\%$
Parasitic Inductance	$\pm 6\%$
Oscillator-Device Impedance	$\pm 15\%$

Design-Centering Error

Design centering is often overlooked as a source of error in establishing the oscillation frequency. To maximize use of the available frequency-tuning range, the tuning limits must be symmetric with respect to the desired oscillation frequency. Any error in establishing this center point, caused by inaccuracies in modeling the components' initial or mean values, reduces the tuning range available to absorb error sources. To guarantee the oscillation frequency over all conditions of temperature, supply voltage, component tolerances, etc., the tuning range must be wide enough to accommodate this error.

You can calculate total frequency error using the frequency-of-oscillation formula, by multiplying each element by a variation scaling factor:

$$f_O = \frac{1}{2\pi\sqrt{L \times C_T}}, C_T = C_V + C_{12},$$

$$C_V = \frac{C_{VAR} \times C_O}{C_{VAR} + C_O}, C_{12} = \frac{C_1 \times C_2}{C_1 + C_2} \quad (8)$$

The quickest way to compute net frequency skew due to the various errors is to utilize a spreadsheet program that contains the detailed formula for oscillation frequency, based on L and C values in the circuit.

Frequency Shifts and Tuning Range

The frequency-tuning range, obtained by varying the tuning voltage from $V_{TUNE(LOW)}$ to $V_{TUNE(HIGH)}$, has high- and low-frequency endpoints (f_{HIGH} and f_{LOW}) with a "center" frequency (f_{CENTER}) defined as the midpoint between f_{HIGH} and f_{LOW} (**Figure 5**). Ideally, the tuning range should be positioned with f_{CENTER} at the desired oscillation frequency (Figure 5a). However, component errors and design-centering errors can shift the frequency-tuning limits.

The desired oscillation frequency cannot be reached if the system provides inadequate tuning voltage over the worst-case conditions, which results in insufficient frequency range (Figure 5b). Clearly, a careful determination of the required tuning range is necessary. That is accomplished by calculating the frequency skew caused by all error sources, and verifying that $f_{LOW} < f_{OSC}$ and $f_{HIGH} > f_{OSC}$ under the worst-case conditions (Figure 5c).

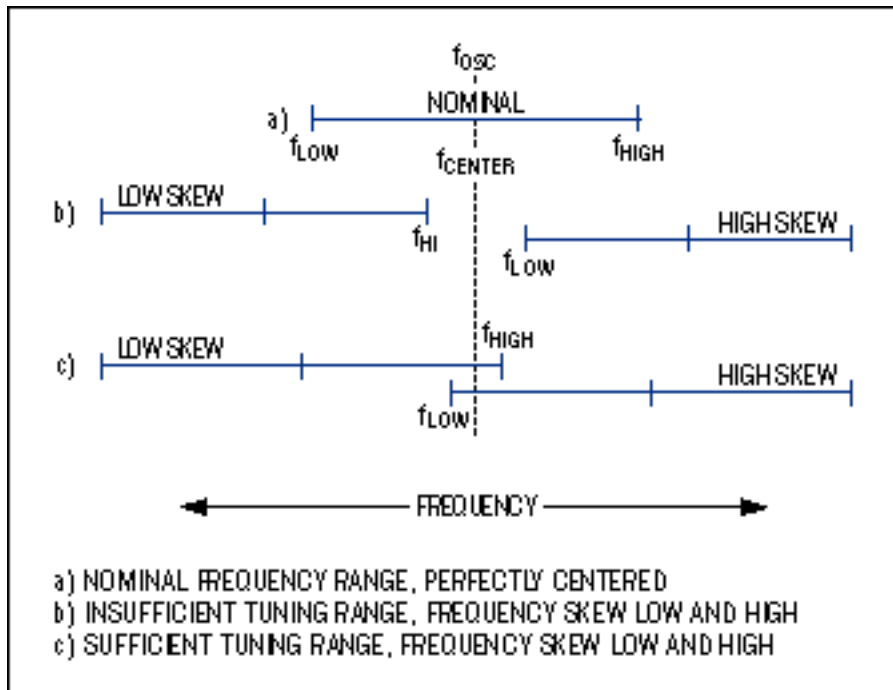


Figure 5. Tuning range and frequency shifts.

Verification of the Design

Once circuit-board layout and component value selection are complete, the design requires verification and measurements (even more than most RF circuits). Nominally, you must check the tuning range, startup behavior, phase noise, etc., for compliance with design targets. In addition, measurements must be made over a statistically significant number of manufacturing runs to determine the tuning range and the mean center frequency, and its location with respect to the desired oscillation frequency.

All this work is necessary to produce a robust, reproducible design with the desired electrical performance.

Because the tasks usually require several iterations, you can easily take months to achieve a discrete-component design that is acceptable and production worthy. Development of a trimless IF VCO requires a detailed circuit design, inclusion of all error sources, verification on the circuit board, and monitoring over production to ensure a viable result. Maxim has met this challenge with a new IC (to be described in Part 2), which solves the VCO design problems while dramatically reducing the time necessary to implement a trimless IF VCO.

Part 2 of this article will introduce the IC, discuss its development, and present a detailed description and performance summary (*Engineering Journal Vol. 40*). An application that illustrates the simplicity, small size, and cost effectiveness of the device will also be included.

References

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2. Hayward, Wes. 1994. *Radio Frequency Design*. Chap. 7.
3. Meyer, Dr. Robert. 1998. Internal communication.
4. Rohde, Ulrich. 1998. *Microwave and Wireless Synthesizers*. Chap. 4.

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